New TOF readout

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Goals:

▷new TOF readout framework has to provide the possibly complete timing and rate information both for online monitoring and offline analysis.
▷The system should contain most of the features of the old TOF readout and monitoring systems.

The following information has to be provided:

- **Trigger bits gated in IA, BG and GL time windows for each TOF/VETO subdetector;**
- **the TDC and rate information for all individual channels;**
- **the hit patterns (e.g. signals gated in IA, BG and GL windows) and corresponding rates for coincidences between pairs of counters;**
- **monitor the stability of IA, BG and GL gates, electron and proton pickups, electron and proton HERA clocks.**

Almost all these features are (and will be) available in the old TOF readout scheme, but:
-the information is spread over 3 different branches, and
-people who have designed and build the system have left.

Implementation:

-Collect all TOF/VETO timing and hit patterns within a single system in room 101.

-Timing from all single channels are digitized by TDC (128 ch. CAEN);
Also all trigger elements for monitoring purpose are digitized by the same TDC.

-All gates, pick-up and HERA clock signals are digitized by TDC (64 ch. CAEN V767).

-"Hit patterns", e.g. gated coincidences are collected by PTL2000 pipeline. Also their rates will be available from PTL2000.

-All single channel rates (except FTI2) will be counted by dedicated scalers (e.g. SIS3801).

-All trigger rates will be counted by PTL2000 scaler.

	PM	Time meas's	single rates	Trigger elements	Gates	Hits
PTOF	4	4	4	3	3	2*3
FIT	8	8	8	3	3	8*3
FTI2	32	32		6	3	2*3
FTI1	16	-		-	-	-
BTOF	8	8	8	3	3	2*3
STOF	8	8	8	3	3	4*3
pickup					2	
H.clock					2	
VETO	22	22	22	3	3	11*3
BTS	8	4	8	12	12	4*3
All		86	58	33	34	33*3
		TDC	*Scalers*	*TDC PTL2000*	*TDC*	*PTL2000*

Hardware:

TOF readout will consists of two independent subsystems:
1) synchronous to H1 readout: TDC, PTL2000-hit patterns- sent via subsystem 101 to H1 data stream and to TOF Slow Control PC.
2) asynchronous to H1 readout: Single channel and Trigger rates- sent at 1 Hz rate to the TOF Slow Control PC.

! no TDC timing measurements if CDAQ/CTrigger are not working !

The readout logic is significantly extended with respect to what was planned before $\longrightarrow$ more custom made electronic modules have to be assembled (NIM$\longrightarrow$H1, NIM$\longrightarrow$ECL level translators, CFD, electronic delays), more cabling to be done between trailer and r.101.

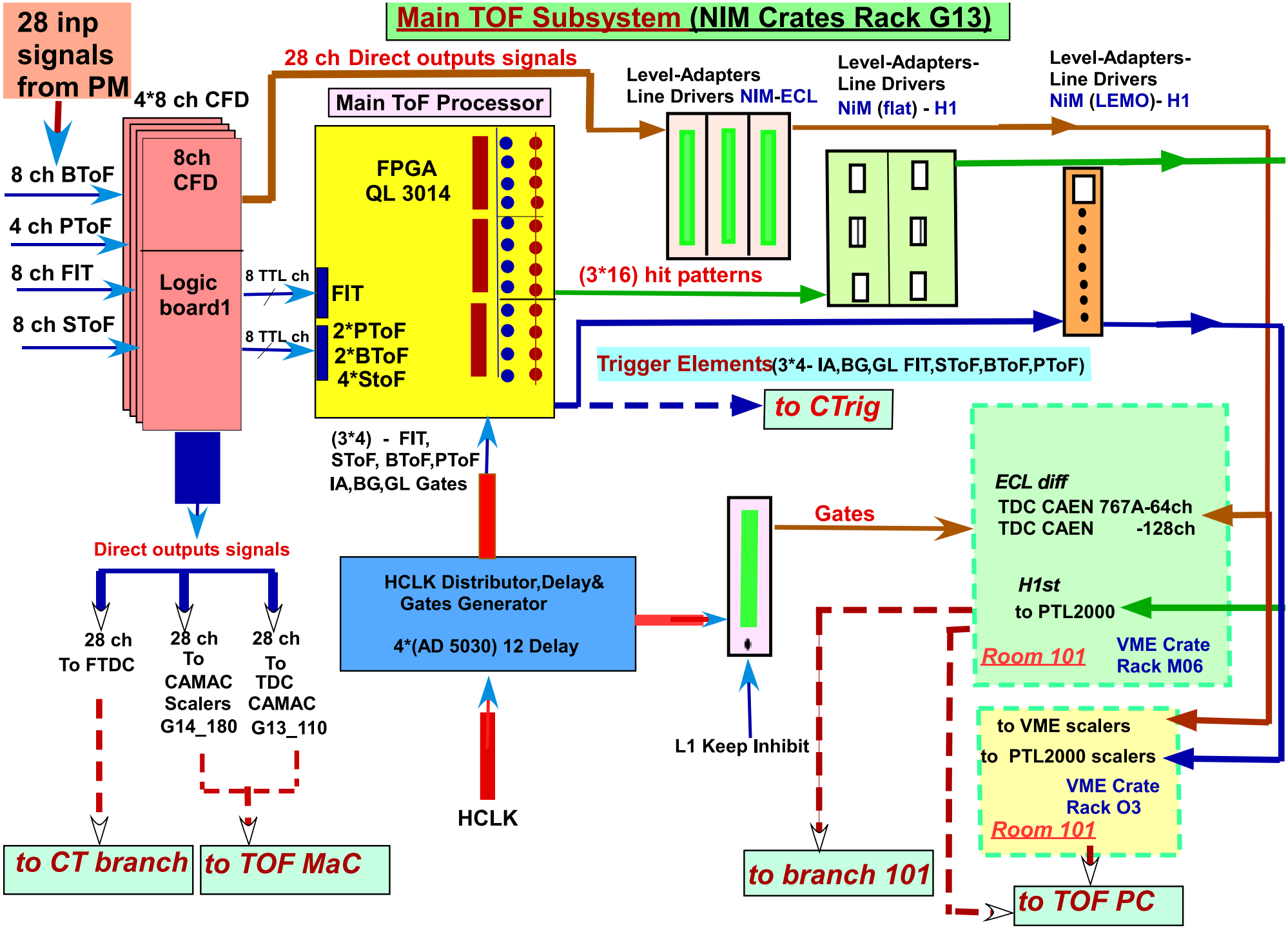
Electronic modules to be purchased/found:
128 ch. CAEN TDC, e.g. V767 or V1190A;
2 $\times$ 32 ch. Scalers (e.g. SIS3801);
I/O register

Software:

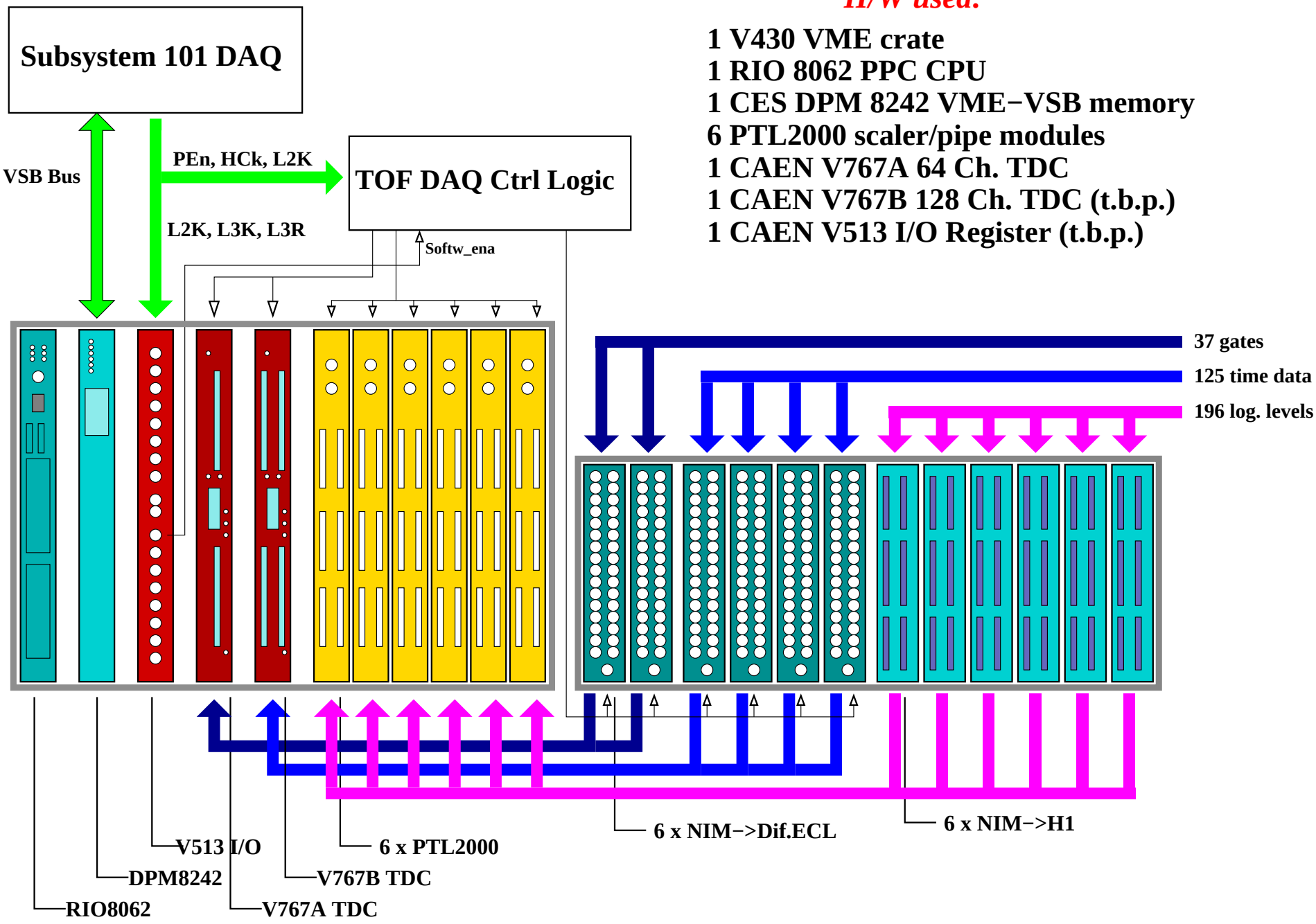
The operation of digitizer modules (PTL2000 and CAEN TDC V767) is tested on real data (BTS and some gates) and in test setup:
-the PTL2000 has shown no big problem up to now (for 3 out of 5 the counting engine is not working – do we have spares ??).
-the TDC operates with glitches: output buffer lockup (known problem), limitation on the incoming hit rate – probably OK for gate measurements, but could be a problem for single hits.

A new version of CAEN TDC 1190A is expected to be free of these problems, but it is still under development, delivery expected by end of 2003. Probably we can still use TDC V767 for single hits, but additional investigations (better with a real beam) are needed.

A new TOF monitoring program is under construction (H.Zohrabyan).


Main TOF Subsystem (NIM Crates Rack G13)
28 inp signals from PM
4*8 ch CFD
28 ch Direct outputs signals
Main ToF Processor
Level-Adapters Line Drivers NIM-ECL
Level-Adapters- Line Drivers NiM (flat) - H1
Level-Adapters- Line Drivers NiM (LEMO)- H1
8 ch BToF
4 ch PToF
8 ch FIT
8 ch SToF
8ch CFD
Logic board1
8 TTL ch
8 TTL ch
FPGA QL 3014
FIT
2*PToF
2*BToF
4*StoF
(3*16) hit patterns
Trigger Elements(3*4- IA,BG,GL FIT,SToF,BToF,PToF)
to CTrig
(3*4) - FIT, SToF, BToF,PToF IA,BG,GL Gates
ECL diff
TDC CAEN 767A-64ch
TDC CAEN -128ch
H1st
to PTL2000
Room 101
VME Crate Rack M06
Gates
Direct outputs signals
HCLK Distributor,Delay& Gates Generator
4*(AD 5030) 12 Delay
28 ch To FTDC
28 ch To CAMAC Scalers G14_180
28 ch To TDC CAMAC G13_110
L1 Keep Inhibit
HCLK
to VME scalers
to PTL2000 scalers
VME Crate Rack O3
Room 101
to CT branch
to TOF MaC
to branch 101
to TOF PC

New TOF readout



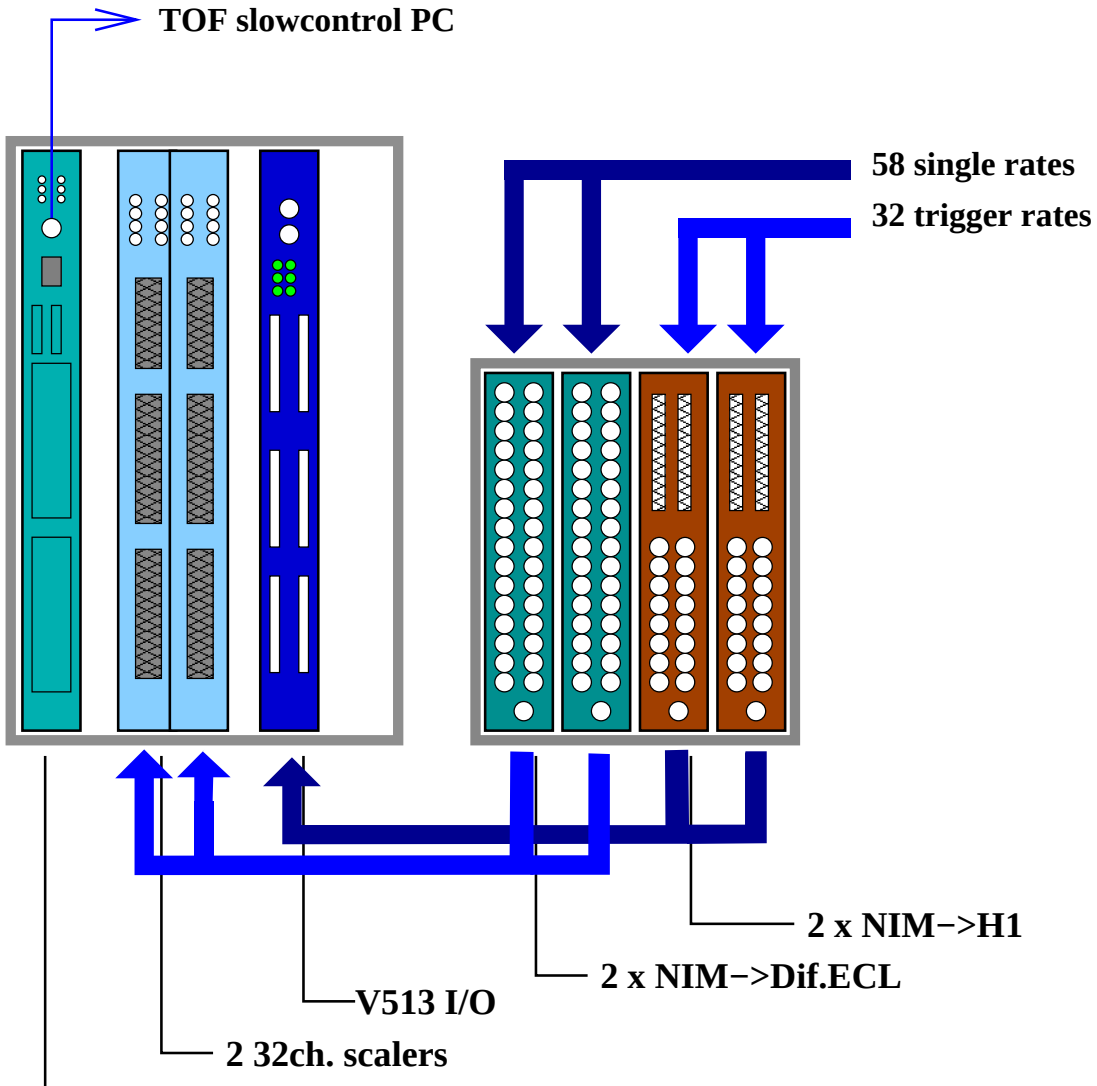
H/W used:

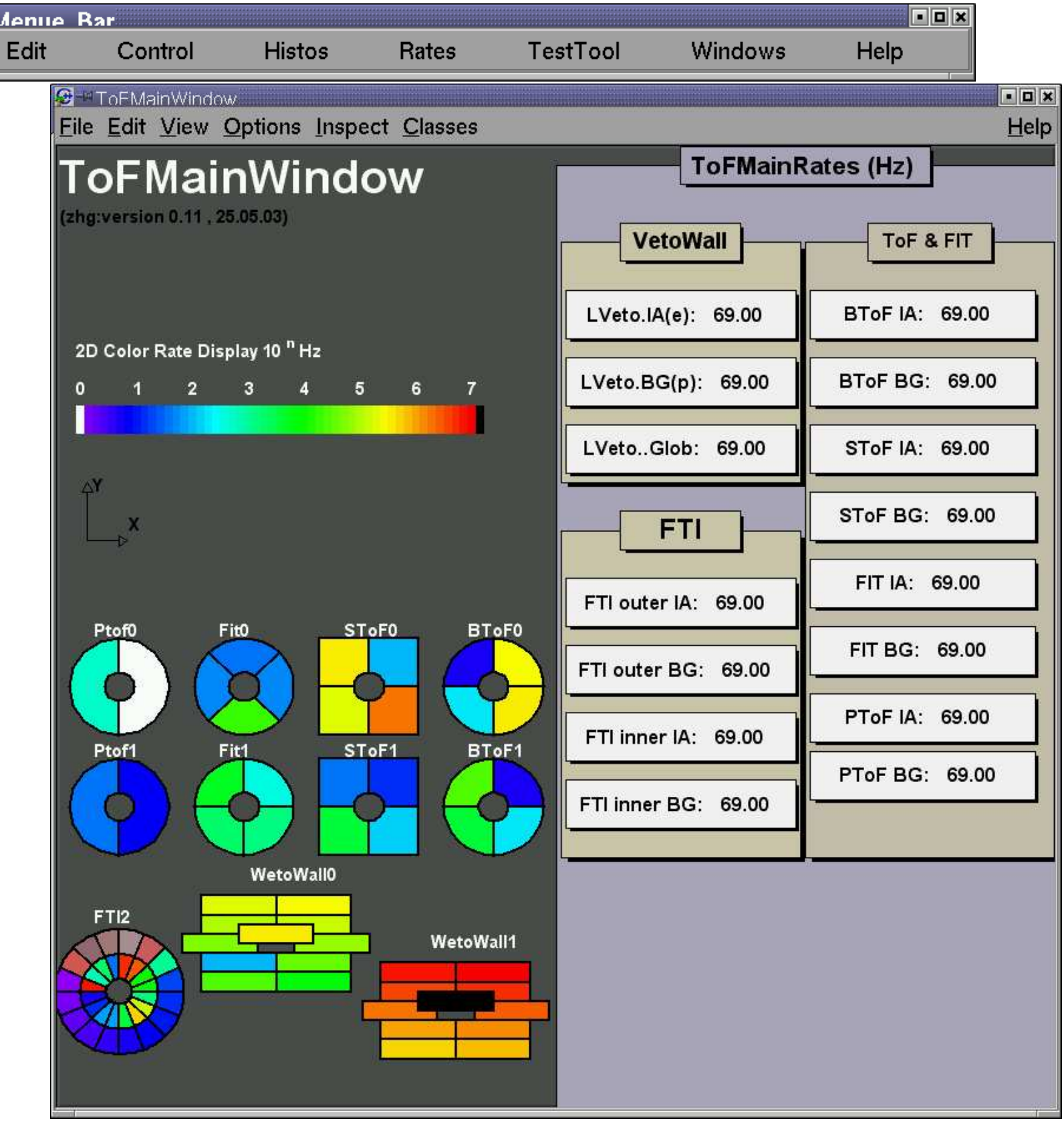
1 V430 VME crate
1 RIO 8062 PPC CPU
1 CES DPM 8242 VME−VSB memory
6 PTL2000 scaler/pipe modules
1 CAEN V767A 64 Ch. TDC
1 CAEN V767B 128 Ch. TDC (t.b.p.)
1 CAEN V513 I/O Register (t.b.p.)

TOF rates

H/W used:

1 VME crate
1 RIO 8062 PPC CPU
2 32ch. scalers (SIS3801)
1 PTL2000 module

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ToFMainWindow
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Help
ToFMainWindow
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ToFMainRates (Hz)
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LVeto.BG(p): 69.00
LVeto..Glob: 69.00
ToF & FIT
BToF IA: 69.00
BToF BG: 69.00
SToF IA: 69.00
SToF BG: 69.00
FIT IA: 69.00
FIT BG: 69.00
PToF IA: 69.00
PToF BG: 69.00
FTI
FTI outer IA: 69.00
FTI outer BG: 69.00
FTI inner IA: 69.00
FTI inner BG: 69.00
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Y
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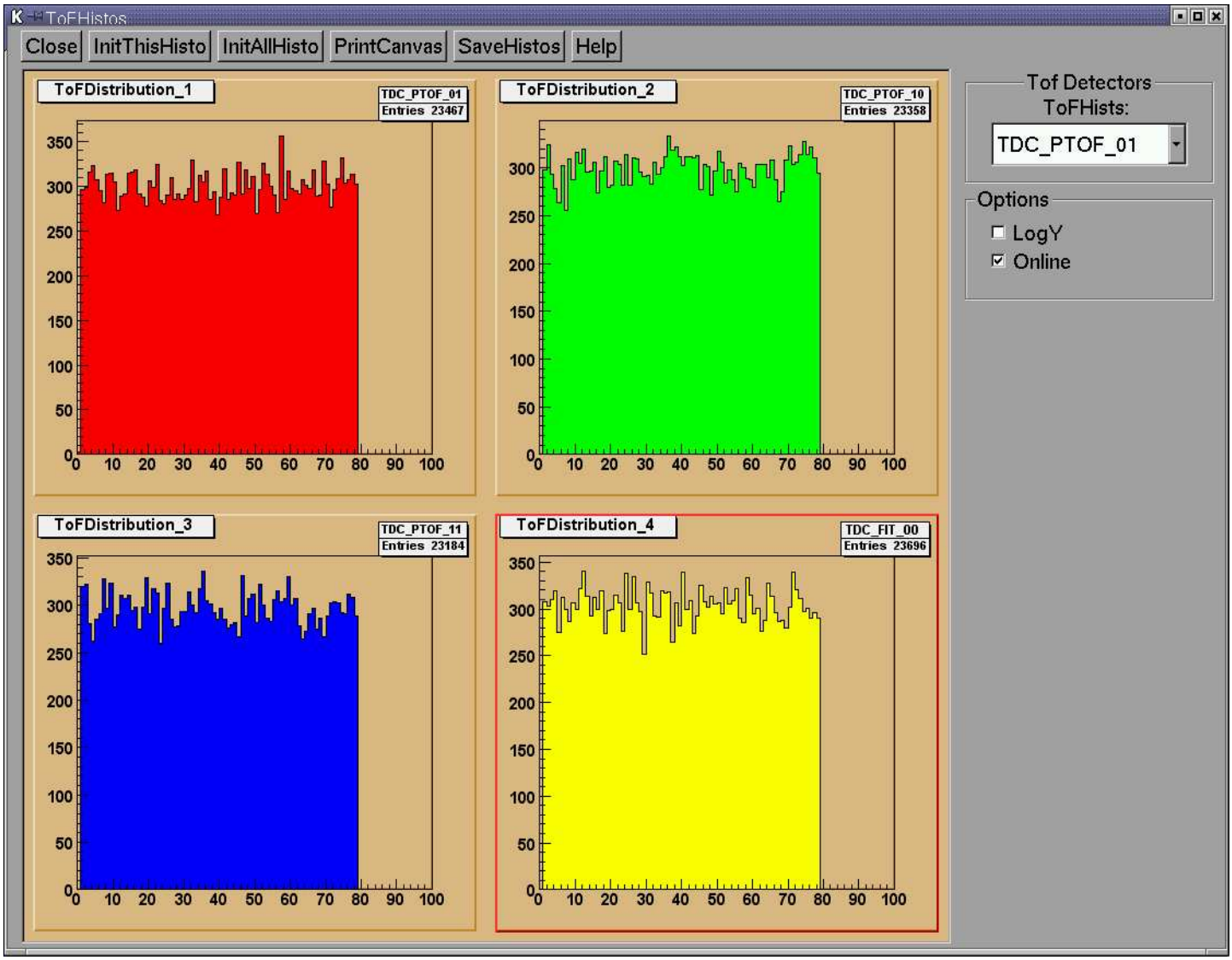
BToF1
WetoWall0
FTI2
WetoWall1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