Contents

Part I.

Techniques and Physics of the H1 Central–μ–Trigger

1. The H1–Detector at HERA

The Hadron Elektron Ringanlage HERA at DESY in Hamburg, Germany, is a storage ring for 820 GeV protons and 27.5 GeV positrons (up to 1994: electrons). At a centre of mass energy of $\sqrt{s} = 300$ GeV, the physics at high momentum transfers of up to $Q^2 = s$ becomes observable. This is of special interest for the evaluation of the proton structure functions [1] and the investigation on the global validity of the Standard Model by searching for new physics beyond, such as leptoquarks or excited leptons [2][3]. In addition, for very low Q^2, HERA can be considered as a charm factory [4].

The difference of the centre of mass system and the laboratory system at the HERA interaction regions leads to an asymmetric design of the detectors. Figure 1.2 shows the detector of the H1 Experiment. In its local coordinate system the proton beam direction defines $+z$. The $+x$ axis points to the centre of the HERA ring. In the following only those of its components will be described in further detail, which are relevant for the studies made. For information on the entire detector and more details on the other subdetectors, the reader is referred to [5].

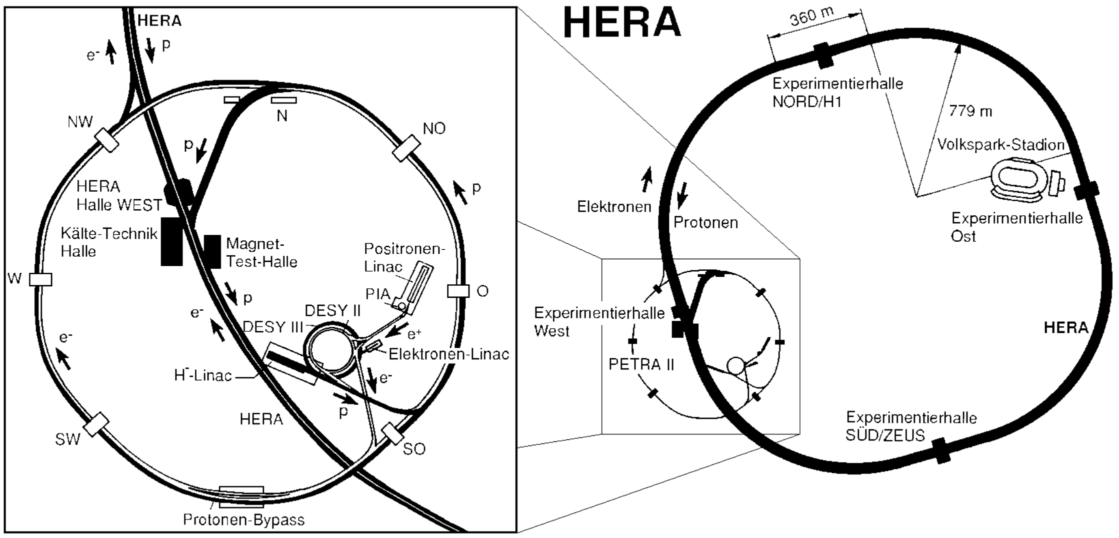

Figure 1.1.: The Hadron Elektron Ringanlage and its pre–accelerators at DESY, Hamburg

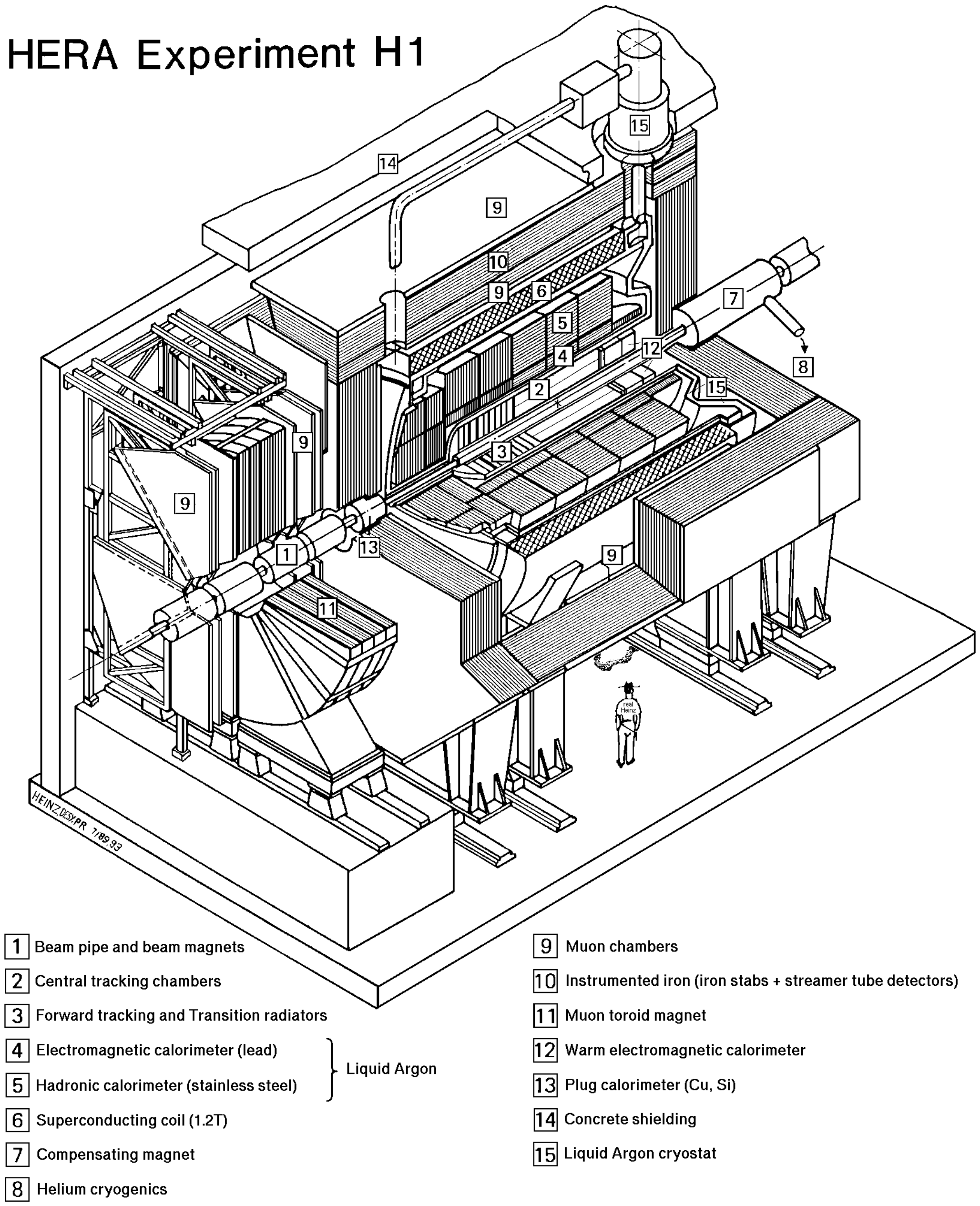

Figure 1.2.: The H1 Detector at HERA

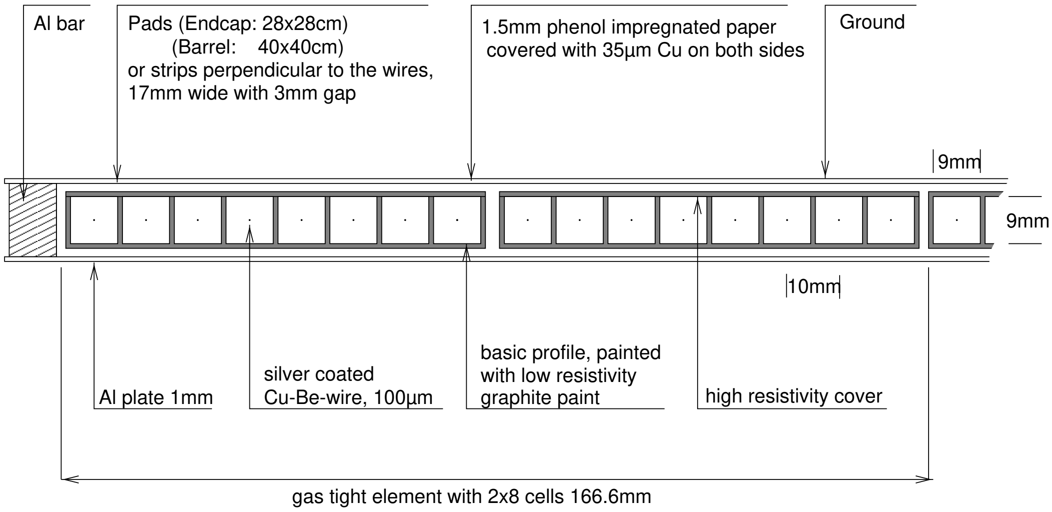

Figure 1.3.: Cut through a Central–μ–LST element perpendicular to the wires

1.1. The Central–μ–Detector

Since high energetic muons are penetrating, as in preceding accelerator experiments, the Central–μ–Detector is the outer most component of the central part of H1 $\boxed{10}$. It is installed in the slits and on the inner and outer surface of the iron yoke of the main H1 solenoid magnet $\boxed{6}$.

The Central–μ–Detector of H1 consists of about 103,000 Iarocci Limited Streamer Tubes (LST) [7] [8]. For safety reasons the LSTs were built of the halogen free plastic Luranyl (©BASF) and are operated with an non–inflammable three–component gas mixture of 88% CO_2, 9.5% iC_4H_{10} and 2.5% Ar. The iso–butane serves as quenching gas to prevent ionisation of the entire LST gas volume which would lead to a fast aging of the chambers. The technical and physical behaviour of the H1 LSTs has been described in various earlier publications [9] [35].

The comb shaped basic unit of the detector hardware, called profile, consists of eight LSTs. Each profile is supplied with HV separately (see figure 1.3).
Two profiles are put together in a gas tight Luranyl box called element (a glossary of all relevant chamber and electronics subdivisions as well as signal abbreviations is given in Appendix A). The chambers are run with the wires at a high voltage of $+4.5\ kV$, which is regulated according to the atmospheric pressure. All connections of supply (gas, high/low voltage) and signal read out are located at one end of such an element. Electrode foils of two types are glued on top of whole layers of elements to collect the charge induced by streamers in the LSTs:

- To enable a measurement of the energy leaking out of the central H1 calorimeters ($\boxed{4}$ and $\boxed{5}$ in fig. 1.2), pads sized $\sim 30 * 30\text{cm}^2$ to $\sim 40 * 50\text{cm}^2$ are installed on the layers, too. They belong to the Tail Catcher Calorimeter (see section 1.6) whose analog readout is assigned to the H1 Calorimeter readout, thus entirely separated from the digital readout of the wires and strips [10].

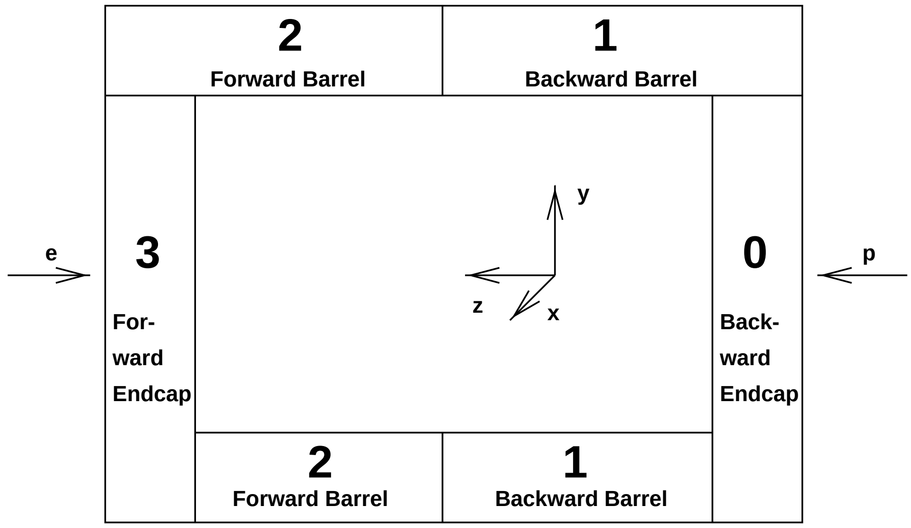

Figure 1.4.: Division of the Central–μ–Detector in μ–subdetectors

- In order get information on the third coordinate of a wire hit, strips of 17mm width are installed perpendicular to the wires. Their digital read out is similar to that of the wires. Simulations before the installation of the strips have shown that the equipment of three layers is sufficient for an efficient track reconstruction.

In analogy to the construction of the H1 iron yoke the Central–μ–Detector is subdivided into a Backward and Forward Endcap (BEC and FEC) and the central part, the so called Barrel (BBa and FBa) (see fig. 1.4). These four parts of the Central–μ–Detector (μ–subdetectors) and are further subdivided into 16 detector modules each (figure 1.5). In the Barrel this is equivalent to half an octant, the Endcaps are divided in each eight modules along the y–axis on either side of the beam. For special purposes it is useful, to number the μ–subdetectors backward to forward from 0 to 3 and the modules within them from 0 to 15 (local module numbers).
The acceptance of the Central–μ–Detector and the position of the modules in the ϑ–φ–plane is given in figure 1.6.
To allow access to the inner H1 subdetectors, the H1 iron yoke is composed of three parts: the northern and southern H1 half-shells and the detector base. Combined with the division into μ–subdetectors, this suggests an administration of the chamber supply with gas, high and low voltage, but also the readout and trigger data processing into five hardware clusters A to E. The assignment of modules to such a logistical cluster is also shown in figure 1.5.
Layers of LST elements fill the $\sim 2.5\ cm$ wide slits between the ten iron slabs of the yoke. Each three layers in an Al box are installed inside and outside the iron. A layer in the iron consists of five elements in the Endcaps, seven to nine elements in the Barrel and up to 14 elements in the μ–boxes. The wire orientation in the Endcaps is perpendicular to the beam (z–) axis, in x direction, whereas in the Barrel it is parallel to the beam.

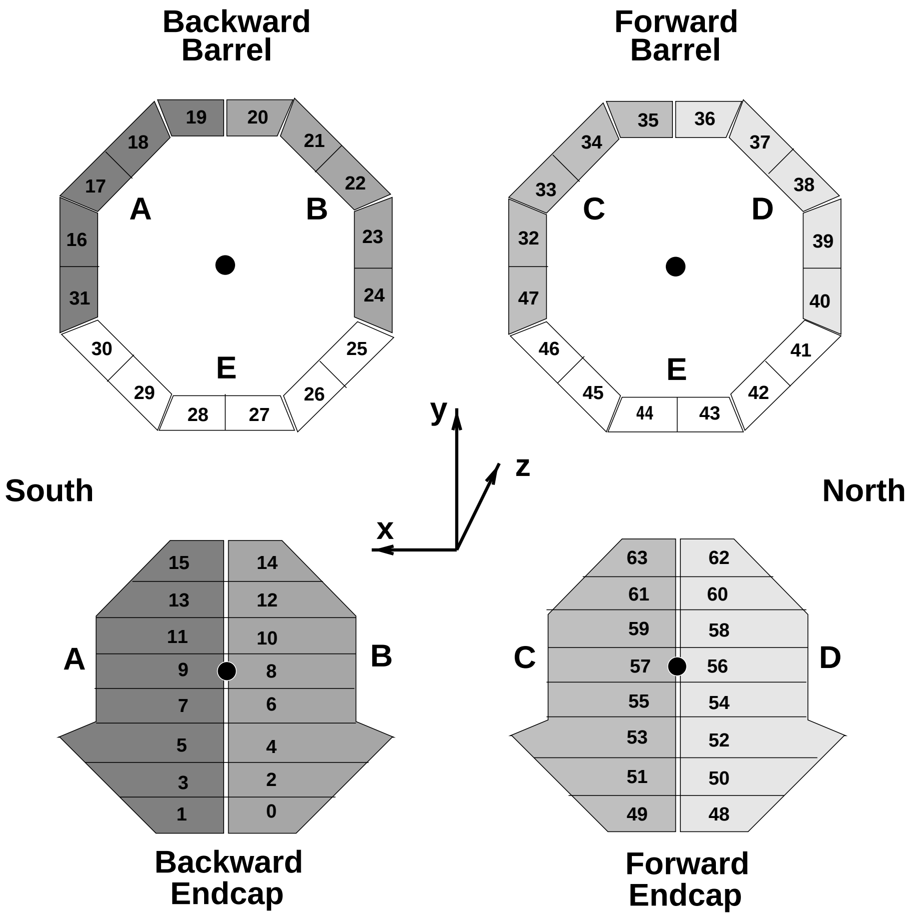

Figure 1.5.: Division of the Central–μ–Detector into 64 modules and their assignment to hardware clusters A–E

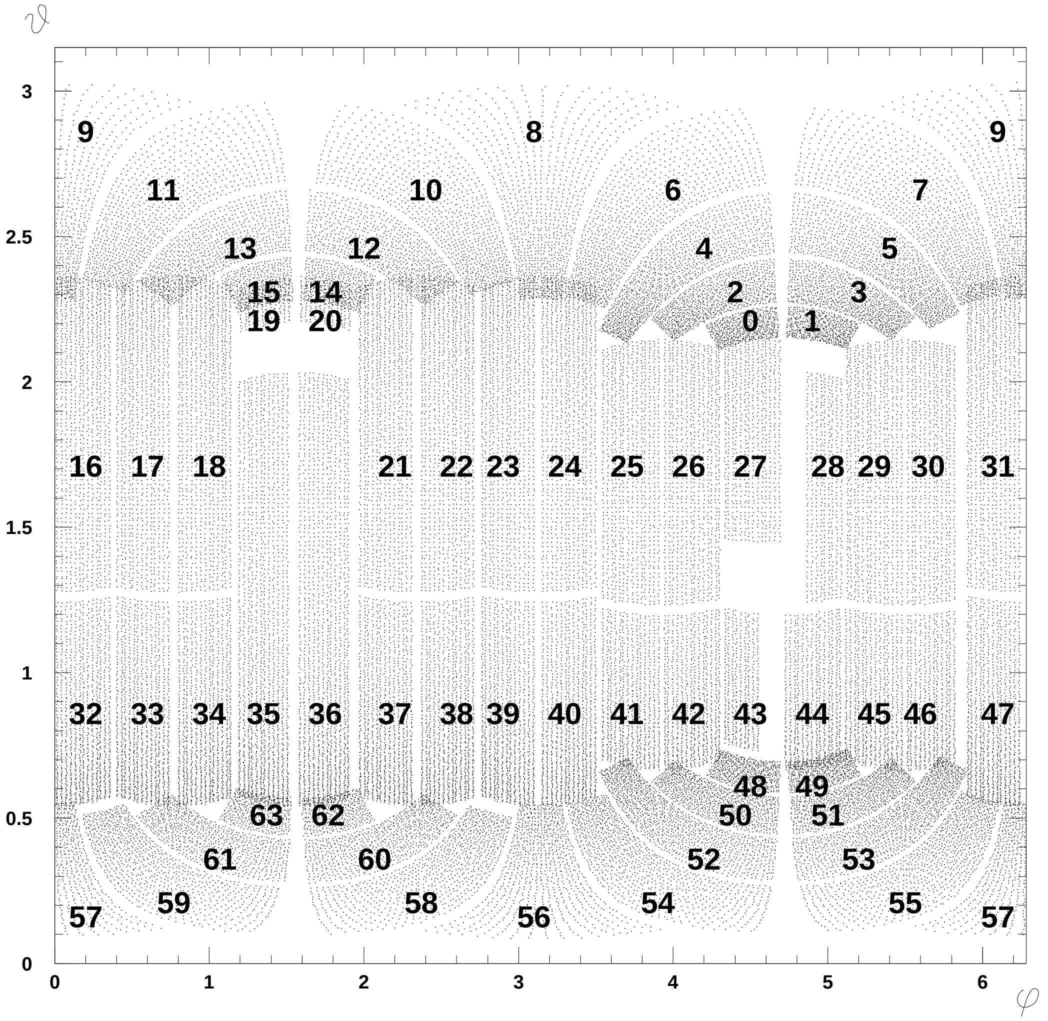

Figure 1.6.: Coverage of the ϑ–φ–Plane by the (iron) modules of the Central–μ–Detector

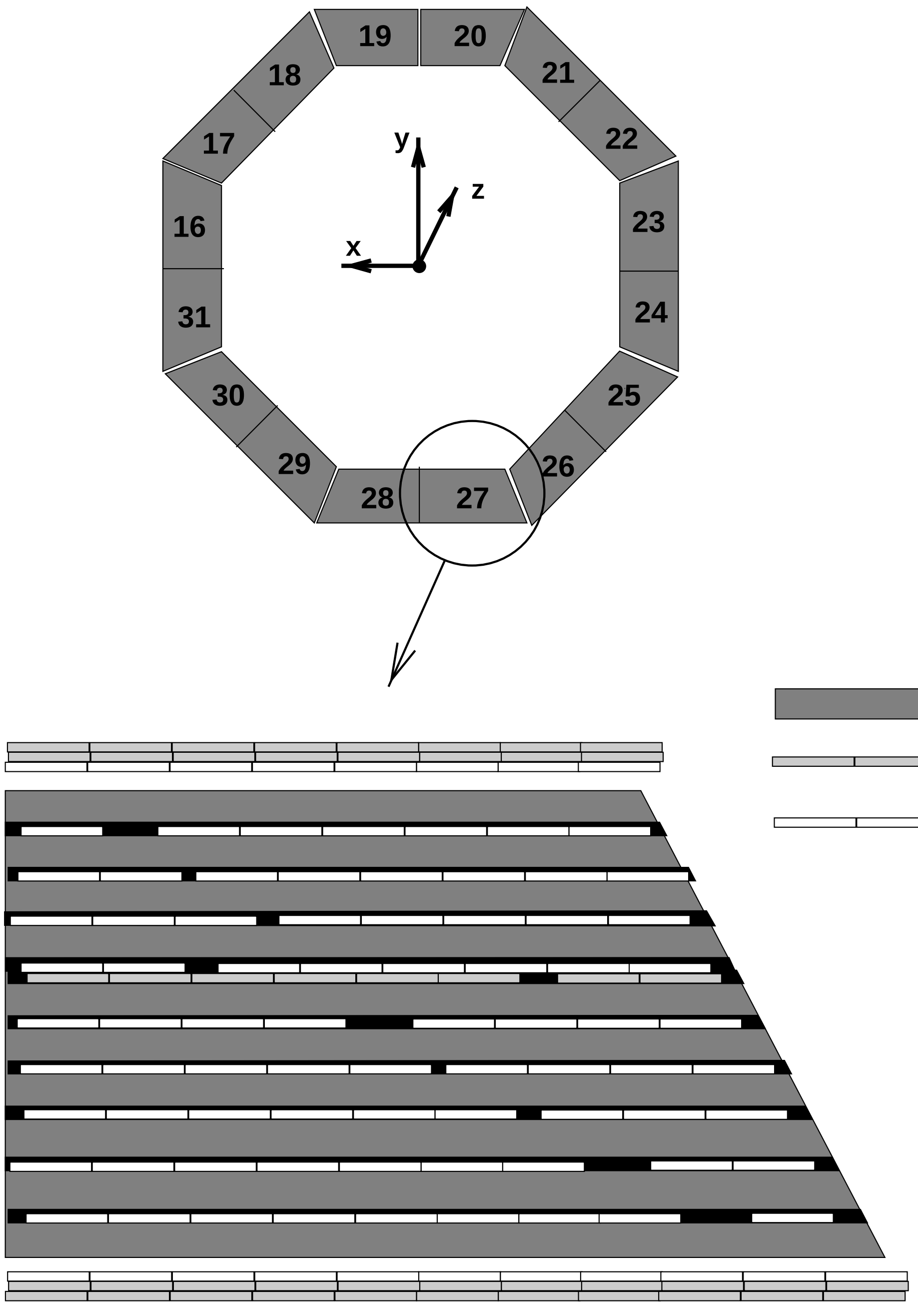

Figure 1.7.: Cut through a module in the Barrel, perpendicular to the wires, showing the different instrumentation of the layers

A cut through a module in the Barrel with the arrangement of strip and pad layers is shown in figure 1.7.
The read out of the digital data from the wires and strips is steered cluster-wise by one electronic unit (Read Out Controller (ROC)) per module [1]. The ROCs perform the steering of the Front End electronics which is installed directly to the LST–elements (see

[1]Since the μ–boxes partly cover regions in two μ subdetectors, some are assigned to module i but read out by ROC j. In the data available offline, this is mapped back.

section 3.1). The ROCs collect the information from the wires, perform a zero suppression and transmit the data to the next level of processing, the Cluster Processors. They prepare the data to be transmitted to the master processor, the Coordinator Processor, i.e. the data is encoded in a form already similar to the raw data bank transmitted by the Coordinator to the Central DAQ [10].

1.2. The Forward Muon Spectrometer

The purpose of the Forward Muon Spectrometer (figure 1.2 $\boxed{9}$, around $\boxed{11}$) is the detection of charged particles which penetrate through the iron yoke of the main H1 solenoid at polar angles $3° < \vartheta < 17°$. These are mainly muons with a momentum $5\ GeV < p < 200\ GeV$. The lower limit is due to the material muons from the interaction region have to traverse to reach the detector and the influence of multi–Coulomb–scattering in the H1 iron yoke on the detector resolution. The upper limit is the consequence of the achievable spatial resolution of the used drift chambers at maximum field of the toroid magnet (figure 1.2 $\boxed{11}$) i.e.

$$dp/p \sim\ 24\% \quad \text{for} \quad p = 5\text{GeV} \quad \text{and} \quad dp/p \sim 36\% \quad \text{for} \quad p = 200\text{GeV}$$

The iron toroid consists of eight semicircular steel modules with an inner radius of 0.65m and an outer radius of 2.9m. It is 1.2m thick and can be opened for access to the beam pipe. The field is provided by twelve rectangular coils (15 turns of $11.5 \times 11.5\text{mm}^2$) of copper tube through which the cooling water flows. The field strength varies from 1.75T at the inner radius to 1.5T at the outer radius.

The Forward Muon Detector is composed in a sandwich structure of three double layers of drift cells on either side of the toroid magnet. Two layers of drift cells mounted on an Al frame build a double layer.
The characteristic data of the drift cells are collected in table 1.1:

# Cells(Wires)	1520
Wires	40 or 50μm Nichrome
Cell Length	$40 - 240$cm
Cell Height	2cm
Cell Width	12cm

Table 1.1.: Characteristics of the Forward Muon Detector drift cells

The cells are staggered by half a cell width to resolve left–right ambiguities (figure 1.9). This divides the detector into active regions of 6cm width and additionally allows measuring the interaction time t_0. The determination of ϑ and φ from the measurement of the drift time is supplemented by a charge division analysis by comparing the read out signal at both ends of a sense wire. The read out is realised with FADCs, clocked at 104MHz into a pipeline with a depth of 256 timeslices. With a φ–layer between the two ϑ–layers on either side of the toroid (figure 1.8), the emphasis lies on the resolution in the polar angle ϑ. The chambers are run at a drift voltage of 3kV across the distributing resistor

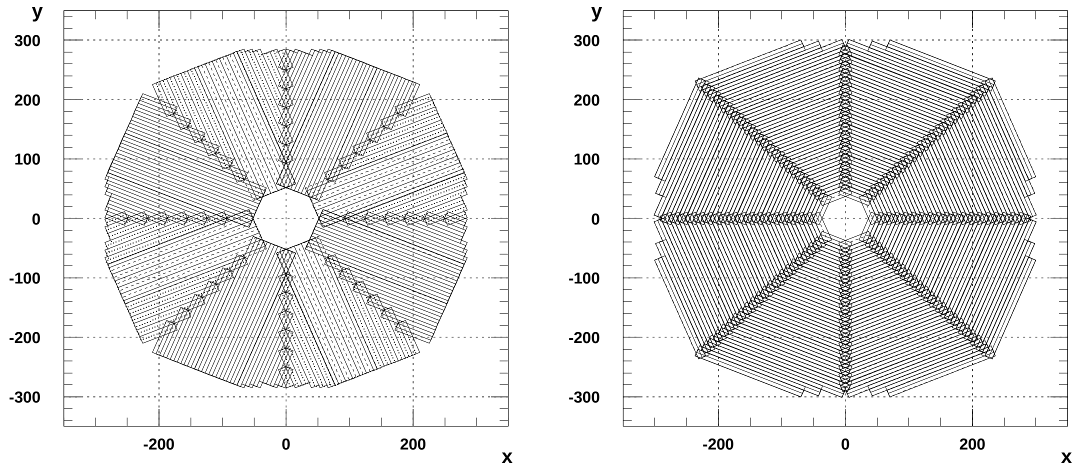

Figure 1.8.: Geometry of a φ– and a ϑ–double–layer of the Forward–Muon–Spectrometer

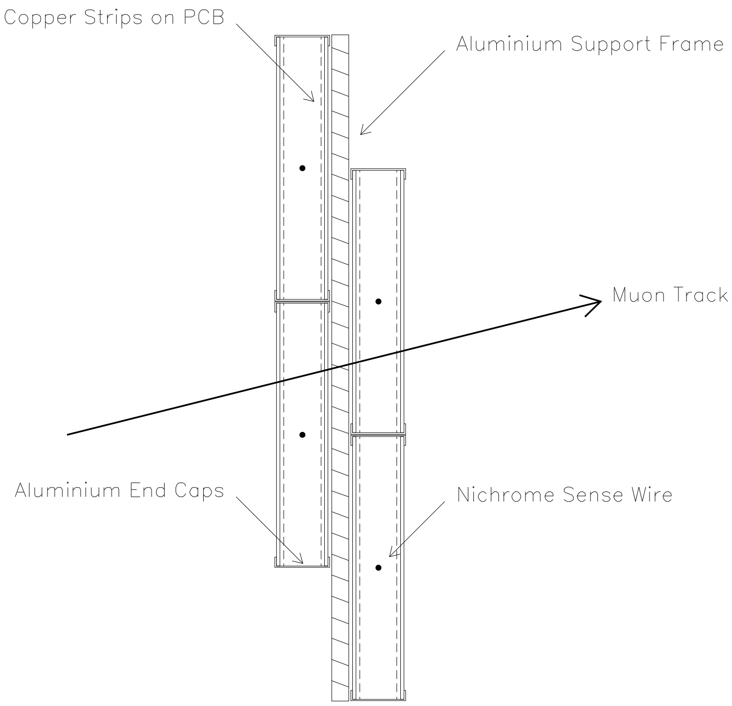

Figure 1.9.: Cut through cells in a double layer of the H1–Forward–Muon–Spectrometer

chain and a sense wire voltage of 4.5kV. The gas is a non–inflammable three–component gas mixture consisting of 92.5% Ar, 5% CO_2, 2.5% CH_4, and is operated in closed system mode. These parameters lead to an average drift field of 0.45kV/cm and constant drift velocities $v_{drift} = 5\text{cm}/\mu s$.
For the present thesis the Forward Muon Spectrometer was used for triggering muon events from the beam halo and to determine the time of the virtual interaction, the t_0 of these events [14].

1.3. The Central Jet Chambers

The track reconstruction in the central region of H1 is based upon the hits in two large concentric jet drift chambers CJC1 and CJC2 (figure 1.2 $\boxed{2}$). They cover a polar angle range $15° < \vartheta < 165°$. The chambers consist of a layer of anode sense wires parallel to the beam between two planes of cathode wires shaping the drift field. The inner ring consists of 30 cells with 24 sense wires each, while the outer ring is divided into 60 cells equipped with 32 sense wires (figure 1.10).
A space point is measurable with a resolution $\sigma_{r\varphi} = 170\mu$m in the drift coordinate ($r - \varphi$ plane) and, by charge division measurements with a resolution of $\sigma_z \approx 22$mm $\sim 1\%$ of the wire length in z.
A tilt angle of the sense wires w.r.t. the r–direction of about 30° allows the resolution of the usual drift chamber ambiguity by linking of track segments in different cells.
Stiff tracks cross the sense wire planes in CJC1 and CJC2 at least once. From the accurate matching at the crossing the passing time t_0 of the particle is reconstructible with a resolution of $\sigma_{t_0} = 0.5$ns. The track parameters are received from up to 56 points per track, which are derived from the drift time measurements on different sense wires. Due to the magnetic field, only tracks with a transverse momentum $p_T \geq 0.15$GeV will pass through both chambers. The achieved momentum resolutions are $\sigma_p/p^2 \leq 0.01\text{GeV}^{-1}$ and $\sigma_\vartheta = 21$mrad.

1.4. The Forward Tracking System

The Forward Tracker consists of three identical sections which are composed of a planar module, a multi wire proportional chamber (see below), a transition radiator and a radial module. Each planar module consists of three layers of parallel wires which are oriented at $\Delta\varphi = 60°$ to each other. The combination of the drift time measurements from these three layers allow a precise determination of space points. The radial modules consist of wires strung perpendicular to the beam axis and provide an accurate measurement of φ but only a vague information on r. The transition radiators, consisting of multiple layers of PP–foil serve to improve the electron identification in this region. Charged particles produce soft x-rays when crossing the boundaries of the PP–foils. The x-radiation then is intended to be detected by the radial modules.

1.5. The Multi Wire Proportional Chambers

Between $5° < \vartheta < 155°$ the solid angle seen from the interaction region is covered by multi wire proportional chambers (MWPCs).

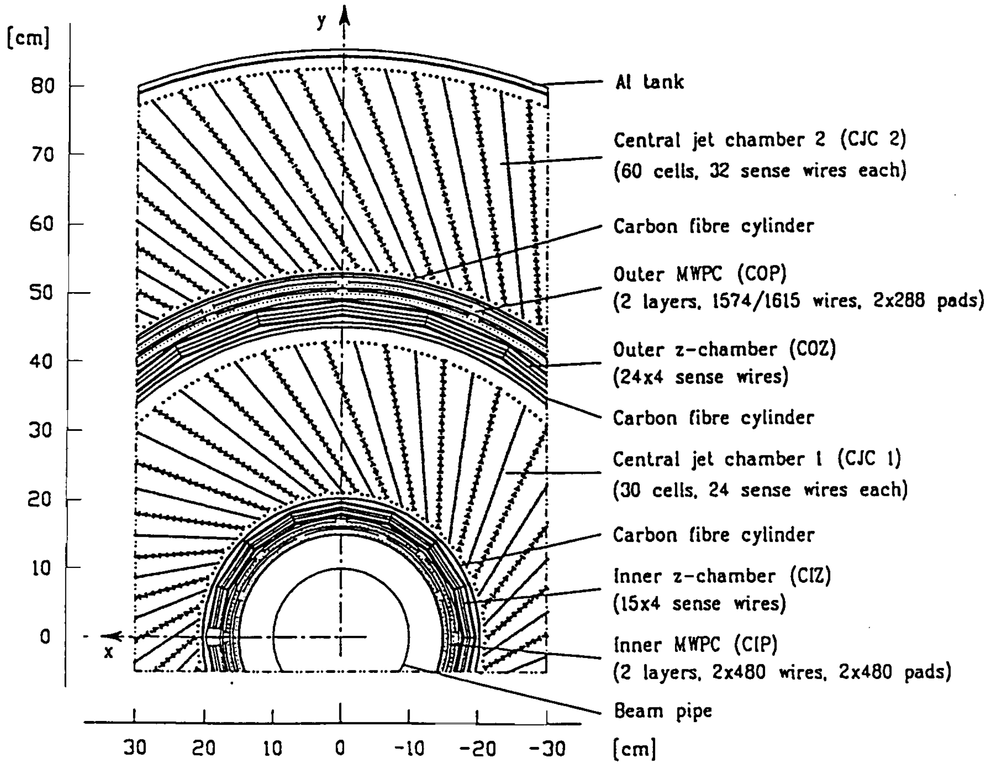

Figure 1.10.: A radial cut through the central tracking detectors perpendicular to the beam.

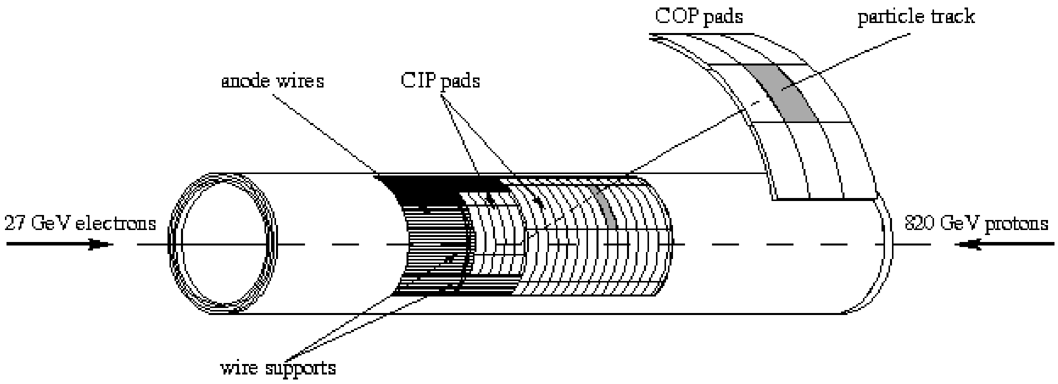

Figure 1.11.: The Central Inner and Outer Proportional Chambers of H1

Six independent planes of the Forward Proportional Chambers (FPC) in the forward direction and four planes of the Central Inner and Outer Proportional Chambers (CIP and COP),as shown in figure 1.10) deliver a fast timing signal with a time resolution better than the separation of two succeeding HERA bunch crossings and provide fairly accurate space points for charged particle track reconstruction at the first trigger level chapter 2). The planar FPC are inter spaced by the drift chambers of the Forward Transition Radiation Detector (see [5]) and are exposed to high particle rates towards the beam pipe.
The central inner proportional chamber (CIP) is closest to the interaction region and covers the largest solid angle ($17° < \vartheta < 156°$ and $0° \leq \varphi \leq 360°$). Since the main purpose of FPC, COP and CIP is to provide space points for the first level trigger, a pad segmented cathode readout was chosen. From the reconstructed tracks the event vertex is deduced. In order to suppress background hits from uncorrelated (electronic) noise and synchrotron radiation the trigger logic requests three or four space points per track. This leads to an angular resolution $\sigma_\vartheta = 0.5$mrad.

The CIP, which is a double layer of chambers consisting of three concentric cylinders, has contributed to this thesis mainly by triggering cosmic calibration data. As electromagnetic shielding, the innermost layer of the first cylinder consists of a 25μm Al foil. For mechanical stabilisation it is glued with a layer of 2mm Rohacell foam by a 20g/m^2 epoxy–glue. The latter is followed by a second Al foil which serves as inner cathode. The anode wires (25μm tungsten) are supplementarily supported at one and two thirds of the chamber length by glasfiber epoxy rings.

The second chamber cylinder serves as outer cathode of the inner chamber layer and inner cathode of the outer chamber layer. Its innermost layer is a 20μm Kapton foil which is coated on one side with a high resistance (400 $k\Omega/\Box$) graphite This guarantees a quick dispension of the accumulated ion charge The other side is coated with 0.5μm Al which is segmented in z into sixty pads of 36mm width in each of the eight φ–sectors which collect the induced charge.
The cathode foils are stabilised again by a shift of 2 mm Rohacell in which the 480 read out wires (150μm Al) run in 250μm deep grooves. They are contacted to the pads by silver paint. An Al coated 20μm Kapton foil glued onto the Rohacell together with the wires is equivalent to a wave guide with a capacitive impedance of $\sim 70\ \Omega$.

The Kapton foil is again backed by 1 mm Rohacell with polished surface and covered by another 25μm Al which serves as outer cathode.

Finally, the sequence of layers of the third cylinder is identical to that of the second.

The chamber are run with gas mixture of 49.9% Ar, 49.9% Ethane, and 0.2% Freon12.

The CIP4 trigger signal (Trigger Element, see section 2.1) used to initiate the read out of the cosmic calibration data, requires two hits in all both layers of the chamber to trigger events back to back in φ . The achieved (test beam) time resolution of 21ns (FWHM) is equivalent to a 2% probability to detect a pad signal in the wrong bunch crossing of the beams.

1.6. The H1 Calorimeters

1.6.1. The LAr Calorimeter

Behind the MWPCs as seen by a particle from the interaction region at a polar angular range $4^\circ < \vartheta < 153^\circ$ the LAr calorimeter is located in a cryostat (see figure 1.2 $\boxed{15}$) inside the main coil of the H1 superconducting magnet.

The inner electromagnetic part of the LAr calorimeter consists of lead absorber plates of thickness 2.4mm between 2.35mm wide gaps in the LAr which is the active material (see figure 1.2 $\boxed{4}$). Per gap, one read out plane with pads and one high voltage plane coated with a high resistive paint with 1-30 M$\Omega/\square$. For the electromagnetic part the barrel region is equipped with three layers of this architecture, the forward region with higher particle rates is equipped with seven 7 layers. This is equivalent to about 20–30 radiation lengths.

The outer hadronic part of the LAr calorimeter consists of 19mm thick plates of stainless steel with independent read out cells inserted between the plates (see figure 1.2 $\boxed{5}$). In the barrel region the hadronic part of the LAr calorimeter is equipped with four layers of the latter construction, in the forward region with six layers. In the barrel this is equivalent to five, in the forward region to seven hadronic interaction lengths.

In z–direction, both parts are divided into eight modules. Each module is divided into eight octants.
The high voltage distribution is done by 1504 independent channels, each supplying several non–consecutive planes to reduce the probability of entirely dead segments.

The LAr energy resolution is about $\sigma_E/E = 12\%/\sqrt{E/\mathrm{GeV}}$ for electromagnetic showers and about $\sigma_E/E = 51\%/\sqrt{E/\mathrm{GeV}}$ for hadronic showers.
The LAr is a non–compensating calorimeter. The charge output of the hadronic part is about $\sim 30\%$ lower than that of the electromagnetic part. For this reason, the shower type has to be determined to enable a correct weighting of the measured energy.

1.6.2. The Tail Catcher Calorimeter

In order two measure the hadronic energy leaking out of the LAr calorimeter, eleven of the 16 LST layers of the Central–μ–Detector are equipped with pads of a size of $(28\text{cm})^2$ to $40 \times 50\text{cm}^2$ as already mentioned in section 1.1 (see also figure 1.7). The pad signals from the inner five (outer six) layers are summed up in electronic devices called tower builders (TB) which provide the front (back) tower signals. The differential analog signals are amplified, integrated and stored in groups of 128 channels in super boards. Information on the Tail Catcher's (TC) instrumentation is given in table 1.2.

region	acceptance	segmentation	# channels
Forward Endcap	$6° \leq \vartheta \leq 33°$	x and y	552
Barrel	$33° \leq \vartheta \leq 137°$	φ and ϑ	2,784
Backward Endcap	$137° \leq \vartheta \leq 172°$	x and y	552

Table 1.2.: Instrumentation of the Tail Catcher Calorimeter

The energy response of the TC for single pions is approximately linear for $E_\pi \leq 40\text{GeV}$ at a resolution $\sigma_E/E \approx 100\%/\sqrt{E/\text{GeV}}$. The energy calibration is done regularly by means of cosmic muons (see also 6.2.2).

1.6.3. The Backward Spaghetti Calorimeter

The H1 SpaCal was installed in the H1 Detector as part of the backward upgrade project in winter 1994/95 [5] and replaced the formerly used Backward Electromagnetic Calorimeter (BEMC) (figure 1.2). The SpaCal is a high resolution lead/scintillating fibre calorimeter which consists of an inner electromagnetic and an outer hadronic section (seen from the interaction region). In 1995/96 the acceptance has been further increased by the installation of a Backward Plug Calorimeter. The characteristics of the SpaCal are concluded in table 1.3.

	Electromagnetic section	Hadronic section
Acceptance	$153° < \vartheta < 177.5°$	
Energy Resolution	$\leq 2\%$at 30 GeV (electr.)	$\sim$40% (hadr.)[12]
Angular Resolution	1-2 mrad	-
Time Resolution	< 1ns	< 1ns
e/π Rejection	>100 [12]	-
Number of channels	1192	136

Table 1.3.: Construction parameters of the H1 SpaCal

The time resolution of <1 ns is achieved by fast shaping units with a peak time of 6 ns by Constant Fraction TDCs.

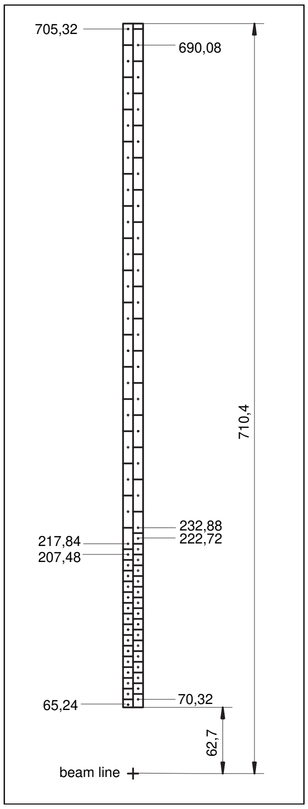

Figure 1.12.: Cut through a BDC double layer octant perpendicular to the wires

1.7. The Backward Drift Chamber

Synchronously with the SpaCal the Backward Drift Chamber (BDC) was installed in the H1 Detector. It replaced the formerly used Backward Proportional Chamber (BPC). The BDC covers the solid angle at $156° < \vartheta < 177°$. Electrons/positrons scattered under very low angles (large ϑ in the H1 convention) are probably detected in the backward calorimeter.
The tasks of the BDC are

- measurement of tracks from the vertex which enter the backward calorimeter with a resolution of about 1 mrad in ϑ.
- identification of electrons which already started to shower up in material before reaching the calorimeter to allow a correction of the measured energy.

To achieve these goals, the BDC was constructed as a sandwich of planes of eight octants each. So eight wires form an octagon around the beam axis which allows a precise ϑ measurement. Two layers with cells staggered by half a cell width make up one double layer (fig. 1.12).
Four of these double layers are installed in z-direction. Each double layer is rotated by 11.25° w.r.t. the previous one. This guarantees that dead areas like cell or/and segment boarders do not line up and prevent a hit in both halves of the double layer. So, each

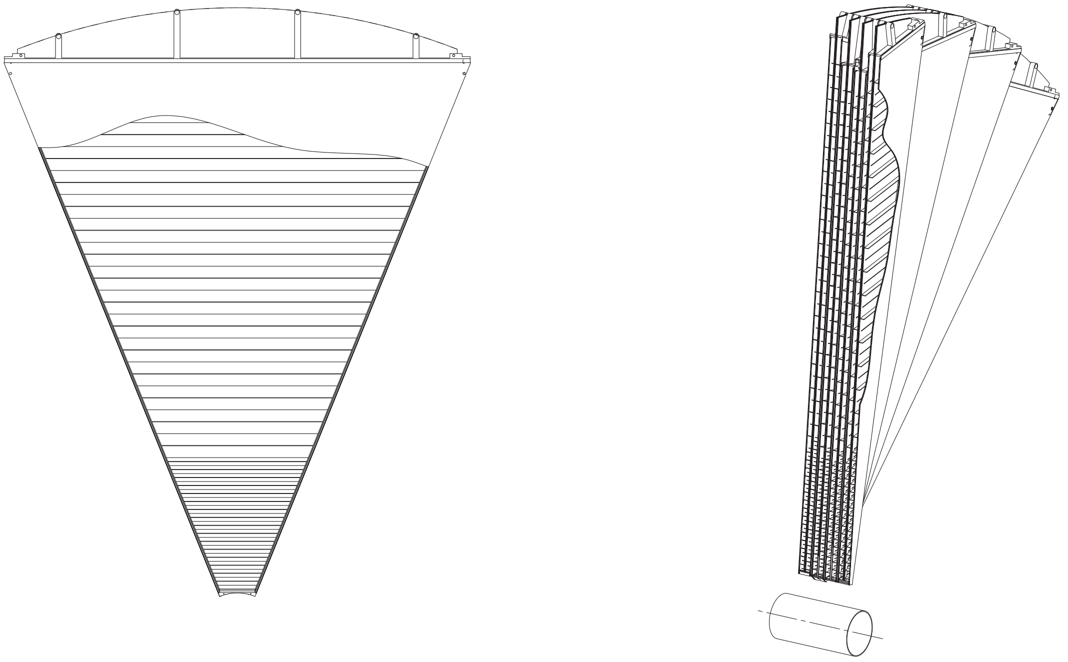

Figure 1.13.: Two different cuts through the BDC

track provides at least six hits in the chamber.
Due to the higher particle densities close to the beam pipe, the inner drift cells are smaller (width 1cm) than the cells in the outer region (width 3cm). So, the maximum drift length in the 16 outer cells ($\sim$ 15mm) is three times larger than for the inner cells ($\sim$ 5mm). At an effective drift velocity of 35μm/ns the maximum drift time is expected to be 450ns which guarantees the arrival of the charge on the wire within a time window of five bunch crossings of 96ns.
Figure 1.13 shows two schematic views of the chamber. In order to measure the drift time and the charge deposited in a cell a FADC readout system analog to that in the other tracking detectors is responsible for the readout of the wire signals.
To reduce the number of FADC channels eight wire signals in a single plane at the same radius are added electronically. This sum then is used as input for one FADC channel. At the same time the signal of each single wire is put into a digital readout chain.
Since both the BDC detector hardware and the structure of the digital data are very similar to that of the Central–μ–Detector , the same electronics could be used not only at the front end but also for the trigger (see section 6.1).
At the digital front end electronics, the analog signals are compared to a threshold value and the digital output of the comparator is sampled with a frequency of 10.4 MHz into a pipeline, as described in section 3.1. The digital readout system has a radial resolution of $\sim$ 2.5 mrad. Since it is very unlikely to observe multiple tracks within this angular range, the digital system can be used to resolve the eightfold ambiguity of the analog information [16].

2. The H1 Trigger Philosophy

The task of the trigger in a high energy physics experiment is the initiation of the readout of the detector. In the Hadron–Elektron–Ringanlage HERA the particle bunches of the two beams collide at a frequency of 10.4 MHz. Therefore, also the period 96ns is called bunch crossing bc. The H1 subdetector read out takes up to $\sim$ 2.5ms, during this time it is impossible to take further data.
Therefore the trigger's additional goal is to separate physics events from background events. One criterium for this distinction is the verification that the detected tracks stem from the vertex region. As a minimum requirement the data of all H1 subdetectors has to be available at the time when the trigger decision is made. For this purpose the signals of most of the H1 subdetectors are digitised, synchronised with the HERA accelerator clock (HClk, symmetric digital clock; period 96 ns), and stored in pipelines.
The depth of these pipelines is different for the different subdetectors. It has to be greater than $\sim$ 23bc, which the Central Trigger Logics Level 1 needs for its decision. Otherwise the data is already lost, when the trigger decision arrives at the front end electronics. Longer pipelines would allow for more elaborate decisions of the first level trigger, but could not be implemented due to economic reasons. Once the first level trigger has fired (L1Keep), the pipelines are stopped. This starts the dead time of the detector. In order to get clean physics data sample at a minimum dead time, for the necessary decisions from stopping the pipelines to storing the data, a multi level hierarchy (L1–L4) had been developed. [17]. A fifth level (L5) performs a full event reconstruction, event classification, etc. offline.
If L1 decides to keep the event, an L1K signal is generated. Each further level n decides to keep (LnK) or to reject (LnR) the input event. The amount and the complexity of the available information is increasing level by level. An LnK is transmitted to the next trigger level L$(n+1)$. L1–L3 take subdetector specific decisions on the data acquisition. On L3K the data of all subdetectors are assembled. L4 decides on the storage of the data to tape. In case of a rejection on level n (LnR), the pipelines, which had been stopped at L1K, are started again by a Pipe Enable signal (PEn). The higher the trigger level, the longer it takes to reinitialise the system to be prepared to accept the next L1K. A Central Trigger Controller performs the communication with the Subsystem Trigger Controllers for each subdetector. This comprises all global steering signals as well as the reception of the respective subdetector trigger signals.

2.1. Level 1

As already mentioned above, it takes 23 bc until L1 decides if for an event the detector is to be read out or not. This is a pure hardware decision, i.e. very fast and free of dead time

but the amount of data available at this time is limited. The H1 subdetectors produce 192 fast trigger signals containing raw information on the energy and/or topology of the event. These signals are called L1 Trigger Elements and are synchronised to the HClk. The TEs are transmitted to the Central Trigger Logics Level 1 (CTL1) for each bunch crossing in groups of eight TEs each (a-p,A-H) (see figure 2.1).
Since this transmission does not happen coincidently for all subdetectors [1], the TEs are individually delayed according to programmable times in a 'trigger carousel'. Such it is possible to synchronise and to combine the TEs from the different subdetectors. In the following step the TEs are logically combined to 128 signals. They are called L1 Raw Subtriggers (L1RSTs). This is realised in an array of static 2k*8 bit look–up table (LUT) RAMs, for which a special Trigger Description Language (TDL) and a compiler have been developed to translate the desired trigger conditions into LUT data.
Several sets of subtrigger conditions can be loaded for different purposes and running conditions e.g. standard e–p running or detector calibration. In addition the TE input can be connected directly to the L1RST output. This is called the transparent mode.
Each L1RST signal can be gated with global option flags. They contain information on the position of the vertex (derived from the MWPC data) and the reconstructed time of interaction, the event–t_0 (from the ToF, LAr, MWPCs and/or the drift chambers).
Since not every fulfilled subtrigger condition is intended to initiate the read out (e.g. high rate physics triggers, monitor triggers), each individual L1RST can be prescaled. This means that at a prescale factor p, the subtrigger is validated only every p–th time it is set. Due to decreasing beam currents (resulting in decreasing raw L1 input rates) a luminosity run is divided into four phases. For each phase a different set of prescale factors is applied. After this validation the L1RSTs are called L1 Actual Subtriggers (L1ASTs). The logical OR of the L1ASTs represents the L1K. (see Appendix B: list of L1 trigger elements and subtriggers in TDL (September 1996), phase dependent L1 prescale factors). The L1K stops the filling of the pipelines and represents the start of the dead time in which succeeding events are lost since the pipelines are stopped. At L1K some subdetectors already start part of the read out (e.g. the Central–μ–Detector starts the read out up to ROC level, see below) and the results are transmitted to L2 [21] [22] [23].

2.2. Level 2

The second level of the H1 Trigger is realised in two different dedicated processor systems. The decision of the L2 Topological Trigger (L2TT) is based on a local correlation of the data from the different subdetectors, mainly by energy clustering in the ϑ–φ–plane. This correlation is realised in Application Specific Integrated Circuits (ASICs) technology [25]. The L2 Neural Network (L2NN) works with 16 two–layer networks with up to 64 neurons per processor which are trained to recognise dedicated event signatures [26].
Each time L1 decides to keep the event, L2 starts to collect the L2 data, which are more detailed than the L1 TE data.
Both L2NN and L2TT provide 16 16-bit encoded values derived from the L2 input data. In case of L2TT they describe the agreement of the event topology to a predefined reference topology. In case of L2NN this represents the significance of the output of the

[1] e.g. the calorimeter preamplifier integration takes up to 23 bc, whereas the FPC and SpaCal data arrive after about 12 bc

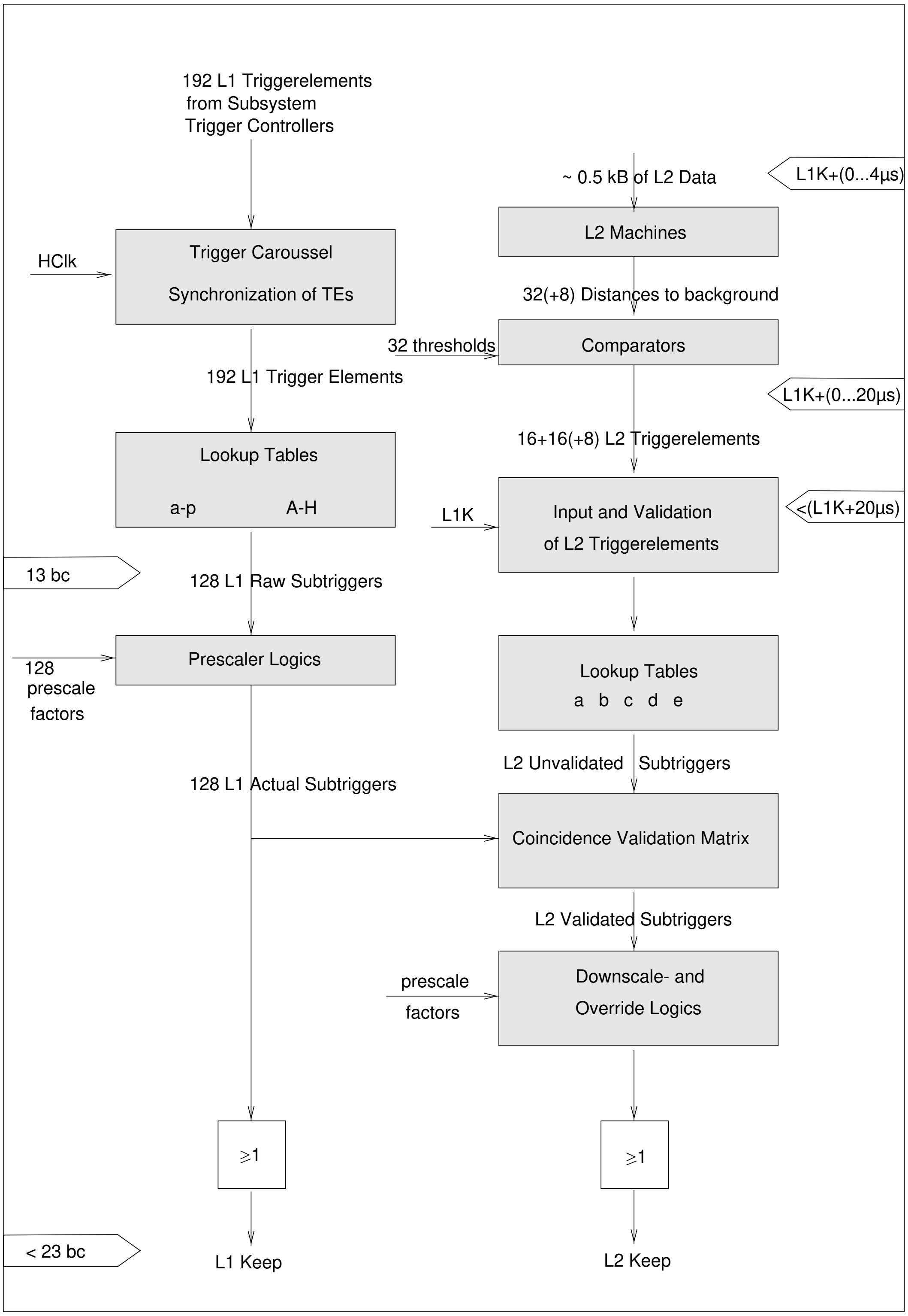

Figure 2.1.: The trigger data flow and relevant times on L1 and L2

network decision. These quality values then are compared to programmable thresholds. The 32 comparator outputs are the L2 Trigger Elements (L2TE) and indicate the presence of a certain signature in the detector (see appendix B).
After a fixed time of $\sim$ 20μs after L1K these L2TEs are latched into an array of 1k*10 bit LUT RAMs. A special unit, called barrel shifter allows combinations of input signals across different LUTs. The 48 LUT output signals are called L2 un-validated subtriggers (L2UST). They have to be validated in a coincidence validation matrix by the 128 L1ASTs. Each of the 48 outputs then is fed into two different validation branches. They are then scaled with two different options to 96 L2 validated subtriggers(L2VST). If at least one of the 96 L2VSTs is set, an L2K is issued, otherwise the event is rejected by L2 [24].
The read out of all subdetectors which already started at L1K, is stopped at L2R immediately. The pipelines are cleared by a Fast Clear signal (FsClr), and are filled again after the subsequent PEn. If at least one of the 96 L2VSTs is set, an L2K is issued, otherwise the event is rejected by L2. L2K starts the read out of all subdetectors (also of those which did not yet started it on L1K) and enables the data is transmitted to L3. [2] A list of the L2 Trigger elements is given in appendix B. Figure 2.1 summarises the (co) operation of L1 and L2.

2.3. Level 3

As mentioned above, a full detector read out takes up to about 2.5ms. If the event is to rejected according to the information available at L3, the L3R signal has to be generated before the completion of the read out in order to reduce the dead time of the detector.
The L3 data of each subdetector are stored (pipelined) in PQZP Store Cards [3] at HClk rate (10.4 MHz) [27]. At L1K the data are sent to the L3 memories via a fast bus system. As other inputs, the trigger elements level 1 and 2 are available as well as a subset of read out data from the subdetectors. The L3 process starts, when the transmission of the data is finished.
The data are analysed by C–programmed algorithms running on a RISC processor. The L3 decision is validated by the Central Trigger Processor (CTP). For monitoring triggers and/or L3 not in use, an immediate L3K is generated. If after 2μs no decision of L3 has been received yet, an L3K is generated by the CTP. Both at L3K *and* L3R the L3 system stop processing and sets its FER. The data of the event accepted by L3 then is sent to the L4 Full Event Memory.
In case of a rejection, the processing is interrupted, no event is built and the CTP sends a Fast Clear and Pipe Enable signal (in this order) to all subsystems which also clears the L3 memories again. The H1 trigger level 3 was not yet in use in 1997.

2.4. Level 4

The fourth H1 trigger level consists of a farm of 38 RISC processors with a total processing power of $\sim$ 650 MIPS.

[2] e.g. for the Central μ detector, the read out is continued i.e. data in the ROCs is collected by the Cluster processors and from there sent to the Coordinating processor in the STC.
[3] Parallel Quickbus Zero suppression Processor

They process the event data asynchronously to all previous trigger levels immediately after they entered the H1 Full Event Memory, to which all processors have access. The Full Event Memory is filled continuously by the Data Acquisition (Event Builder), which collects the data from the Multi Event Buffers (MEBs) of the subdetectors and composes the event. The MEBs of the subdetectors are connected by a glass fibre taxi ring [28].
The farm processors perform a partial event reconstruction with the H1 reconstruction software package H1REC. This comprises the Qt analysis for the drift chambers, (central) track fitting, calorimeter clustering, checking for energy cuts and vertex selection as well as the rejection of primary background events such as beam gas and/or beam wall events. This leads to a raw data reduction of about 80% and the decision if the event will be written to Raw Data Tapes or not. A small fraction (about 1%) of events is always kept for monitoring reasons. L4 in principle performs a dead time free parallel multi event processing. This is not the case anymore if the number of events to be processed in parallel becomes too large or if the amount of data submitted by selected subdetectors is so large that the reconstruction takes much longer than foreseen. The critical rate $R_{crit.}$ for the latter case is determined by the average L4 processing time per event $\langle t_{L4} \rangle$ and the number of L4 processors $n_{\text{L4-Processors}}$:

$$R_{crit.} = \frac{n_{\text{L4-Processors}}}{\langle t_{\text{L4}} \rangle} \sim 30 \text{ Hz} \quad (1995/96) \tag{2.1}$$

This rate of course will increase with more and/or faster processors, which will be installed during 1997 [30]. Since t_{L4} depends on the event topology and size, the L4 output is not necessarily ordered chronological.

2.5. Level 5

The fifth and final level of the H1 trigger is an offline trigger which processes the Raw L4 output data saved on disc. L5 is intended to process the L4 output data directly after they have been written to tape. The purpose of L5 is the final preparation and filtering of the data to an exclusively physical extract.
The least requirement for an event to written to Physical Output Tapes (POT) or Data Summary Tapes (DST) is at least one active physics L1AST. This filtering is performed on a 16 processor mainframe computer with 6*2 GB disc space and 1 GB RAM [4]. On all 10 processors identical copies of the H1 event reconstruction software package H1REC are running in parallel. The event data are collected and delivered by two event server processes. The L5 output events are sorted by run/event number, they are completely reconstructed, physically classified and written to POTs. A subsample of the data volume for each event is stored on DSTs.
The average L5 processing time is $\langle t_{\text{L5}} \rangle \approx 1$ s [18]. Thus, at good terms the entire L4 output data can be reconstructed within a few hours after they have been taken.

[4]disc space extended in August 1997 to 3*9 GB + 3 * 2 GB

3. The Electronics of the Central–μ–Trigger System

The decision to derive and use a fast trigger signal from the digital wire hit information at all was made after the installation of the chamber hardware. Since during the design of the chambers and the electronics the emphasis lay on an efficient and precise read out, one had to cope with constraints growing from the chamber and electronics design, which are described in detail in chapter 5. The following chapter describes the trigger electronics involved from the generation of the initial fast trigger signals from a streamer set in an LST to the final production of Central–μ–TEs which are transmitted to the CTL1. Figure 3.1 shows the flow of the Central–μ–Trigger data from the Front End Read Out to the Central Trigger Logics Level 1 (CTL1).

On this way through the different electronic modules the data is reduced from about 33,000 single wire signals used for the trigger to eight TEs (figure 3.2).

3.1. Initial Generation of fast Trigger Signals on the Wire Digital Module Boards

The analog signals from the 16 consecutive LST wires in an element (= two profiles) are directly fed into the primary front end read out electronics of the Central–μ–Detector , the Wire Digital Module Boards (WDMBs). They are connected to the LST elements at their supply end and provide digitisation, synchronisation to the HClk and pipelining of the analog streamer pulses for the digital read out [6]. In addition, the synchronised digital signals are available at the input of the pipeline and used to derive a fast trigger signal. Each analog wire signal is digitised (and converted to TTL) in the comparator circuit shown in figure 3.3a. The digitisation threshold voltage (0 – 255mV) is provided to the WDMBs modulewise by programmable Digital to Analog Converters on the Readout–Controllers (ROCs) which also provide other major steering signals (see [10]).
At PEn active, the digital signals from one profile enter a custom made ASIC on which in a first step they are synchronised to the HClk (figure 3.3b). In this dead time free circuit, in which the (p)reset is only used for test purposes, the length of the digital signals is fixed to 96 ns (1 bc) (compare Appendix D). The HClk is provided only while PEn is active.
Before the signals then enter the readout pipelines, which are 32 bc deep, in both gate–arrays the 8fold OR of the input wire signals is built. These two signals are provided directly as a fast trigger output, either separately or as a 16fold wire OR signal (selection

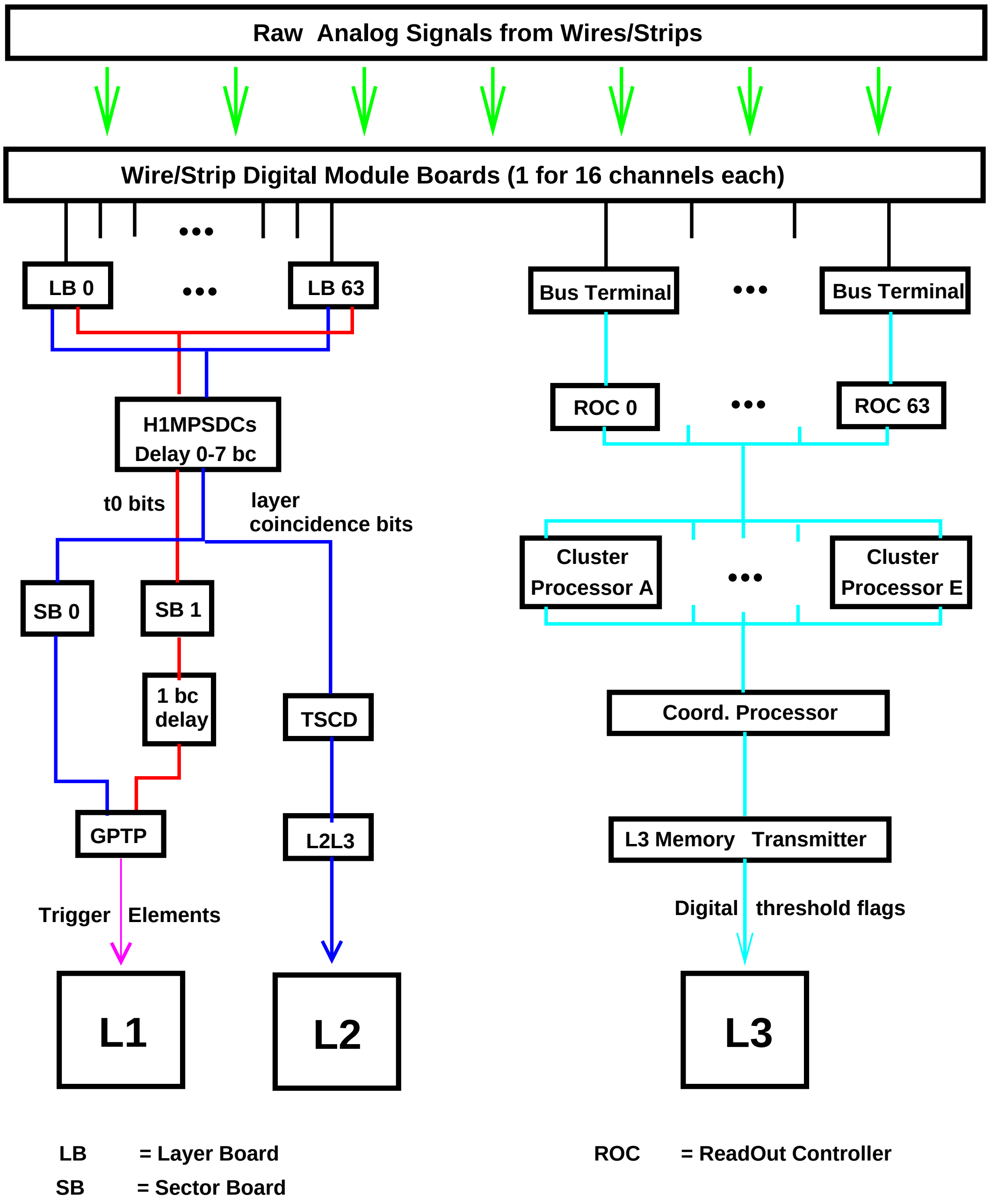

Figure 3.1.: The trigger data flow from the chambers to L1, L2, L3

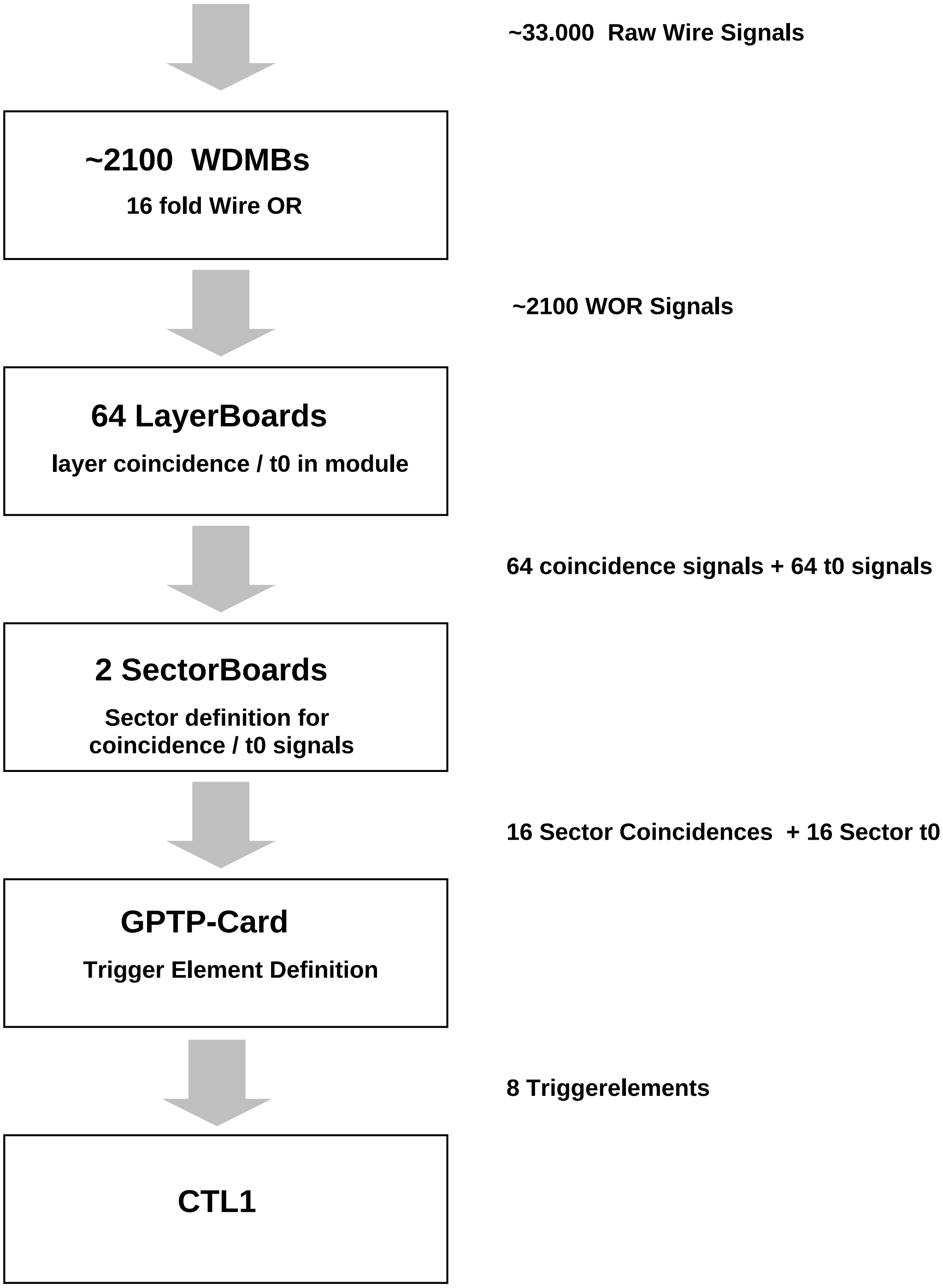

Figure 3.2.: The reduction of the L1 trigger data from the Central–μ–Detector

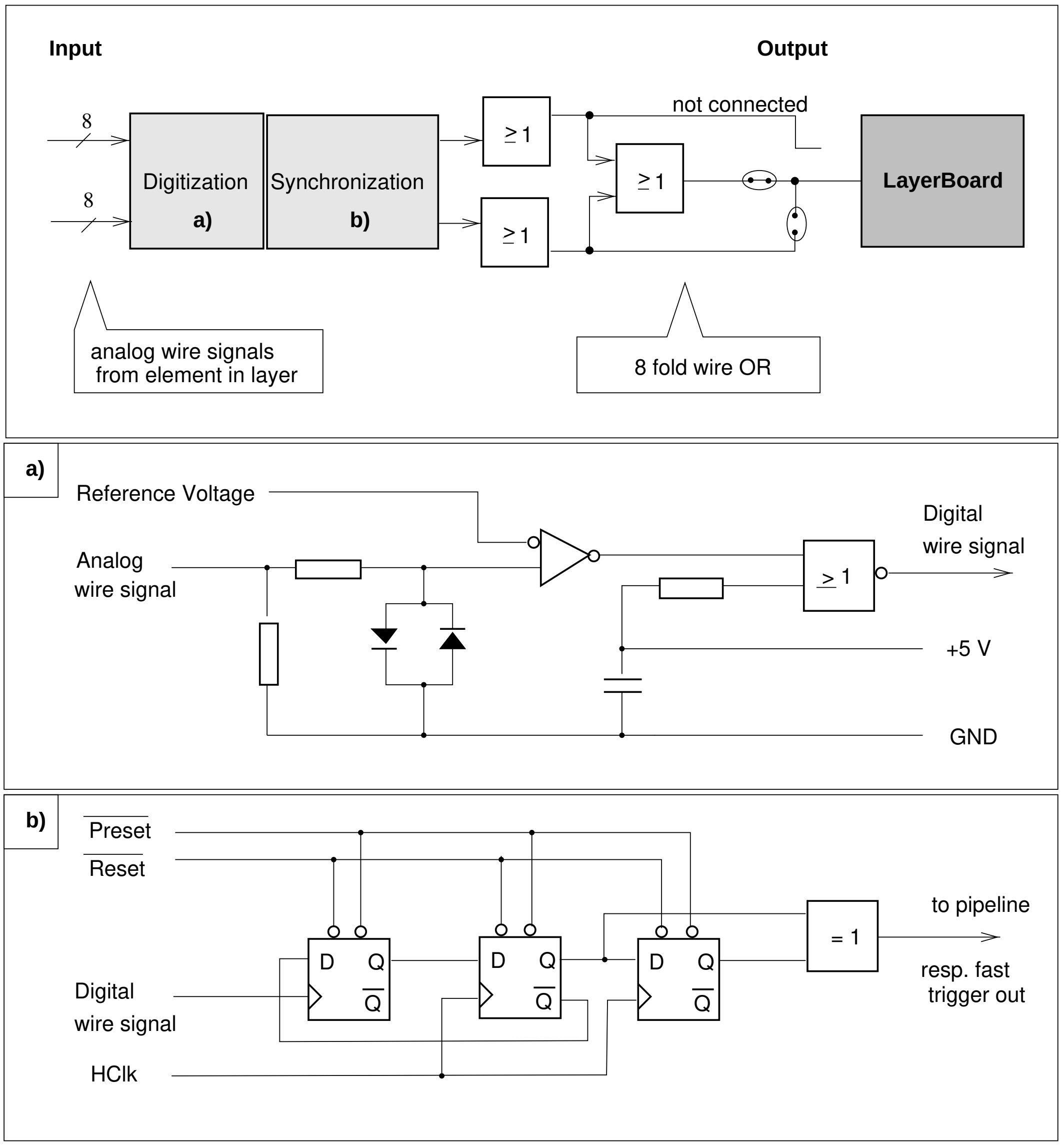

Figure 3.3.: Scheme of the WDMB functionality

via jumper setting). The latter signal, which is used for further processing, will be called WireOR (WOR) from now on. Before transmission to the next level of processing, the WORs are converted from TTL to RS422A, which always is used to transmit signals between different electronic modules especially for long distances. The strip signals are processed analogously in Strip Digital Module Boards (SDMBs) but with three differences:

1. The input signals are pre-amplified before being transmitted into the comparators.
2. The threshold voltage is positive since the signal was induced by the (negative) streamer in the respective LST.
3. The strip signals do not contribute to any trigger decision on L1, L2 or L3.

3.2. Distribution of the HClk by the Clock Receiver Boards

The HERA accelerator clock signal which is used for signal shaping and synchronisation, is distributed cluster-wise to the module individual electronic devices of the read out and the trigger of the Central–μ–Detector . On the trigger side, the HClk signal is received by special boards located in the electronic crates containing the devices processing the WDMB output from each module. On these Clock Receivers the HClk signal is delayable in steps of 1/4 bc. Two derivates of the HClk with a relative phase of 1/4 bc are provided to the devices in the crate via its backplane bus.

3.3. Detection of Layer Coincidences on the Layer Boards

Up to nine WOR signals from five selected trigger layers (compare section 4.2.1) in each module are transmitted to the next level of processing, the Layer Boards (LB). They are intended to detect coincidences of hits in different layers of one module. In total there are 64 LBs installed in the system, one for each module. In a first step the WOR signals from all elements of the same trigger layer in the respective module are logically ORed (figure 3.4). This element OR (ELOR) signal represents the activity of any digital wire signal in the layer. In addition to the ELOR signals from the five trigger layers, two additional bits of information, called majority bits, are produced. They indicate the presence of a hit in more than one element, more than two elements respectively. This feature is foreseen to discriminate shower tails from penetrating muons (see 4.2.3). Some precaution has to be taken w.r.t. the maximum drift–time when aiming for coincidences of some of these seven signals: on the one hand the maximum drift time in an LST amounts to about 140 ns (in detail in chapter 5) but on the other hand the active length of the WOR is fixed to 1 bc = 96 ns (see appendix D). In this construction the detection of coincidences of hits in different layers although originating from the same particle is not guaranteed. Therefore the signals can be artificially stretched to a length of up to 4 bc in steps of 1 bc in programmable shift registers driven by the HClk.
The five ELOR signals plus the two majority signals for layer 3 are transmitted to the address lines of a static 128*8 bit RAM which is used as a look–up table. Thus it is possible to deliver eight output signals per board representing any logical combination of

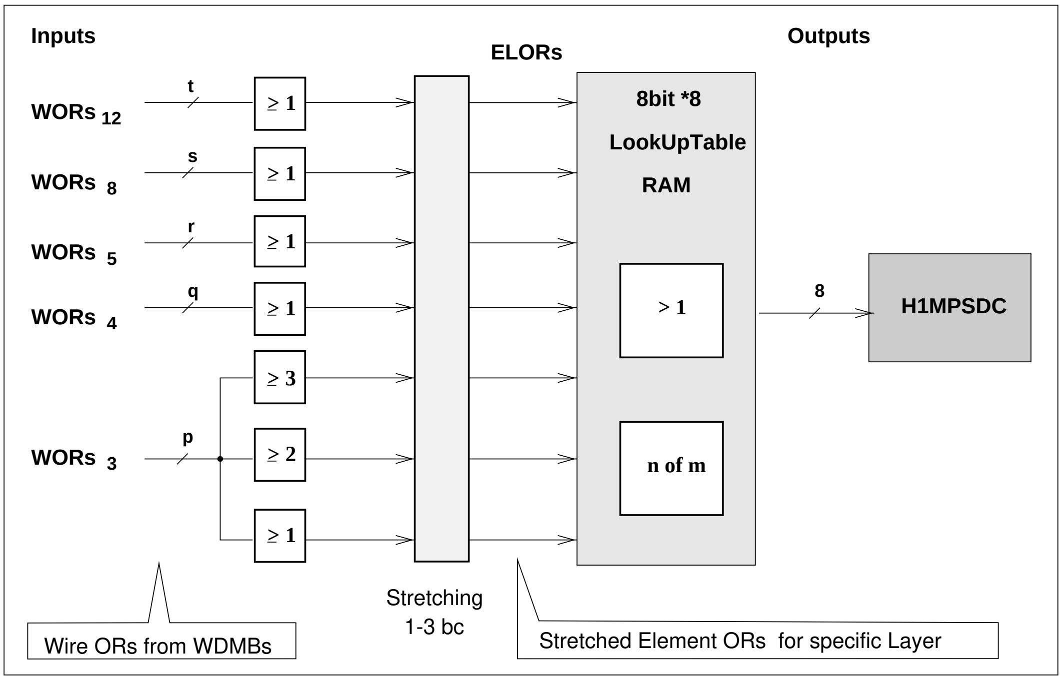

Figure 3.4.: Scheme of the Layer Board functionality (letters {p,q,r,s,t} mean number of elements connected to the input port)

the ELOR signals. Two output bits are used in the experiment.
Since the RAM is gated with the HClk (96 ns period), at each bunch crossing the output pattern is determined by the state of the input signals.
Since the LBs for the modules of the five clusters are installed in non VME–Standard Crates, the RAMs are loaded via a custom made VME interface board, the Filter Memory Loader (FML, section 3.10). This board is accessible from the system supervising Macintosh computer in the control room of the experiment.
On the LB output side, the signals are delayable by 0 to 264 ns in steps of 24 ns (=1/4 bc) to compensate the very different lengths of the cables from the cluster crates to the next level of processing in the experiment's electronics trailer [1]. This allows tuning the arrival of all LB output signals in a way, that their phase w.r.t. the HClk is more or less alike. As will be discussed in chapter 5, a smaller step size foreseen in the design would have supported the optimisation trigger timing.

3.4. Reassignment of Signals on the Patch Panel

As can be seen from figure 1.5, the assignment of modules to the five supply clusters is incompatible with the division of the detector into μ–subdetectors (fig.1.4). For this reason and for reasons of systematic further analysis of data, the LB output signals have to be reordered concerning module/LB number and meaning (i.e. LB output bit). This

[1]This is realised by means of the second HClk derivate provided by the Clock Receivers mentioned in section 3.2.

signal ordering is realised on a printed circuit board, called Patch Panel.Unfortunately, at the same time the latter ordering is also a mixing w.r.t. the timing of signals which were transmitted from the LBs assigned to different hardware clusters. This can result in an assignment of the trigger signal to a different bc after the succeeding resynchronisation step.

3.5. H1 Multi Purpose Signal Delay Card H1MPSDC

This electronic module is again a custom made electronic device ([32]).
The board is capable to process 32 digital signals. Eight consecutive input signals, twelve control signals (one triplet per pair of input signals) and the HClk enter a Complex High Density Programmable Logic Device (CPLD). In the latter circuits the possible variety and complexity of the data manipulation is only limited by the programming capacity. For usage in a standard VME crate, the input is expected from the front connectors, whereas for the usage in the Central–μ–Trigger system, the input is expected from J1.
In the Central–μ–Trigger , one task of the H1MPSDCs is the resynchronisation of the LB output signals before these enter the next processing level, the Sector Boards' RAMs (see section 3.6). This is important for the recognition of signal coincidences, since the Sector Board RAM outputs are resynchronised to the HClk.
The CPLDs are programmed with shift registers with programmable depth (0-7 bc), which is determined by the three bit steering patterns. Each three bit steering patterns is valid for two consecutive CPLD input signals, which are the coincidence and the t_0–signal from one LB. Thus it is guaranteed that the signals originating from the same module are delayed by the same number of bc (see also appendix D). By this technique, modulewise corrections of the timing of the trigger signals are possible, which was not the case before the installation of the H1MPSDCs in the system (see chapter 5).

3.6. Definition of Trigger Sectors on the Sector Boards

Each group of 64 LB output signals which have been processed in the H1MPSDCs is analysed w.r.t. coincidences of module triggers (defined in LBs) in this electronic board. At this level of processing the trigger data still has to be reduced. This can be done in two different ways:

a) The signals are connected μ–subdetector wise to the address lines of four static 64k x 4 bit LUT RAMs. The LUTs define topological sectors by logically uniting several modules, which leads to the name Sector Board (SB).

b) The signals from two consecutive modules in a μ–subdetector are ORed (this means e.g. one signal per barrel octant). The resulting groups of eight signals per μ–subdetector combined with those from a different μ–subdetector in non gated 64k x 4 bit LUT RAMs.

So in total the SB–RAMs are able to provide 32 output signals which are then resynchronised to the HClk. Each signal represents the presence of a certain configuration of the input module trigger signals. The RAMs again are loaded via the same interface module as the LB RAMs. The SB output is converted from TTL to RS422A again to be transmitted to the General Purpose Trigger Pipe Board (GPTP) via twisted pair cable.

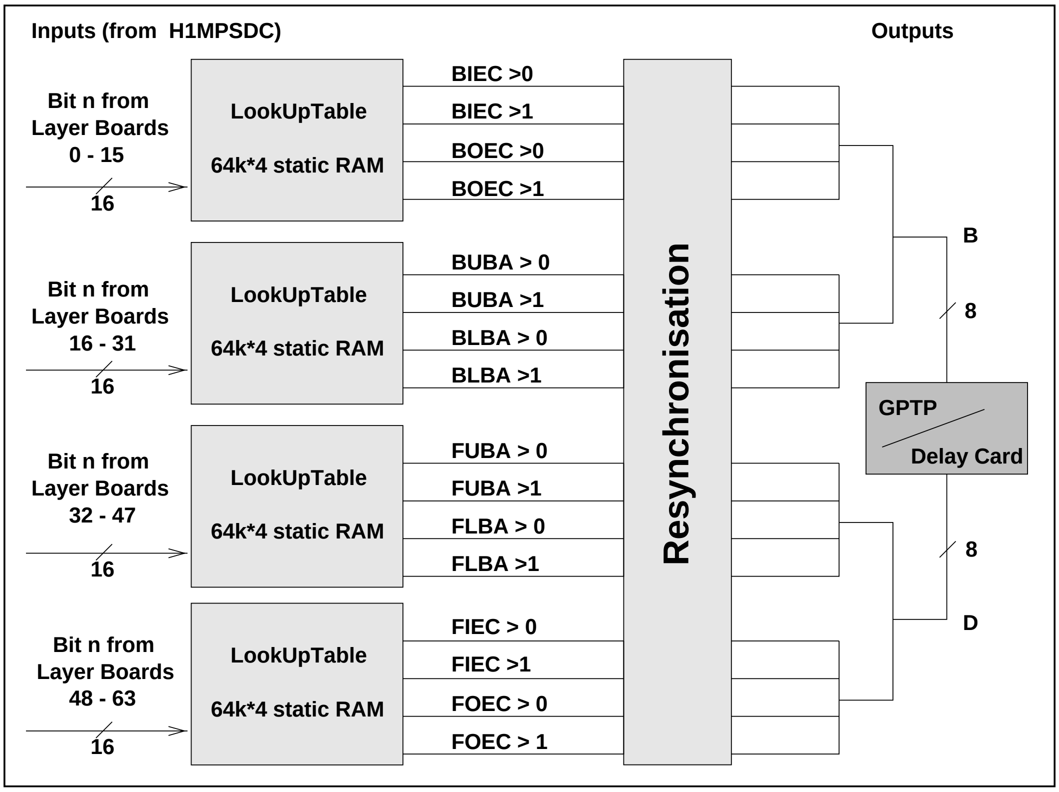

Figure 3.5.: Scheme of the Sector Board functionality

3.7. Delay Card for Sector Output Signals

The sector t_0 signals (the output of the SB processing the LB-t_0 signals) are delayed by one bc w.r.t. the sector coincidence signals, before they are transmitted to the GPTP Board. The reason for this delay is explained in section 4.4.1.

3.8. GPTP Board: Definition of Muon TE for L1

The final electronic module in the chain the Central–μ–Trigger data has to pass, before they are transmitted to the CTL1 is the the General Purpose Trigger Pipe Board (GPTP). It is the H1 standard electronic device generating the Trigger Elements and is used in most of the subdetector trigger systems.

The GPTP is able to process 32 digital signals which are connected in groups of 8 signals to four input ports A–D (figure 3.6). For monitoring purposes, all 32 input signals are stored in a 32 bc deep pipeline which is driven by one of the HClk signals supplied with the incoming data. The data in monitor pipelines are read out by the Central–μ–DAQ and contribute to online monitoring histograms filled on the L4 filter farm.

In parallel, the data pass a (software programmable) AND/OR gate, in which the signals entering ports A and B (C and D) are combined bitwise.

The resulting two groups of eight signals then pass a delay pipeline with a programmable depth to adjust the arrival time of the final trigger elements at the CTL1. The position

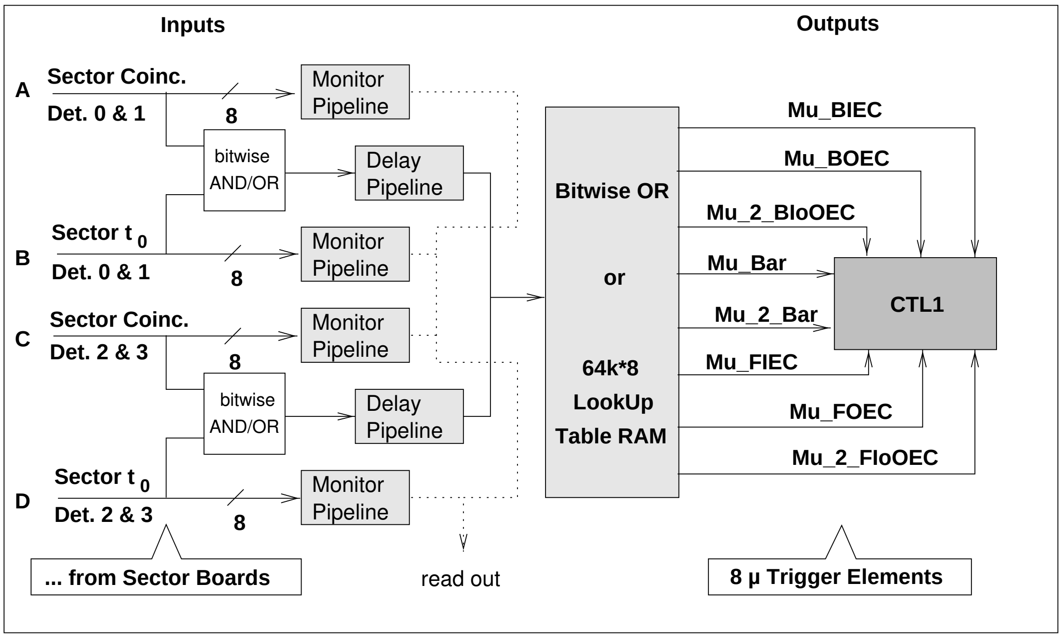

Figure 3.6.: Scheme of the functionality of General Purpose Trigger Pipe Board

of the data in the latter delay pipe determines the bc in which they are received at the CTL1. The appropriately delayed trigger signals then either build the address bits of a static 64k*8 LUT RAM or are bypassed through a (hardware) bitwise OR. The LUT RAM is loadable from the Central–μ–Detector 's supervising Macintosh computer in the H1 control room directly via VME.
The resulting eight signals represent the contribution of the Central–μ–Detector to the L1 Trigger Elements.

3.9. PQZP Store Card: 64 module triggers for L2

In parallel to the processing of the LB output signals in the Sector Boards, the layer coincidence signals from the 64 Central–μ–Detector modules are transmitted to the PQZP Store Cards of the L2/L3 system and enter a pipeline with a maximum depth of 32 bc. On L2 and L3 only the data in the interaction bc (t_0 bc) is analysed. For this reason the bc in which the signal becomes active it is not so important. It only has to be guaranteed that the trigger signals are still/yet active in the bc transmitted to L2/L3 [27].

3.10. Filter Memory Loader Board

Since the Layer– and Sector Board crates do not fulfil the VME standard [39], an interface from VME is necessary to load the look–up tables into the boards' RAMs. It is accessed via a software application running on a Macintosh computer in the experiment's control room which controls both the trigger and the data acquisition of the Central–μ–Detector (see appendix F). The Filter Memory Loader Board (FML) is a custom made VME

I/O board based on a VME–Prototyping board [20]. The Layer– and Sector Boards are controlled by one FML each. Therefore a design had been chosen with 5 Output ports (for 5 clusters max.)
The LUT RAMs of the LBs and SBs are loaded in 8 bit serial mode driven by the VME strobe clock. Figure 3.7 shows the timing of a write cycle for writing a 1, a 3, and a 7 (from left to right) to the SB.

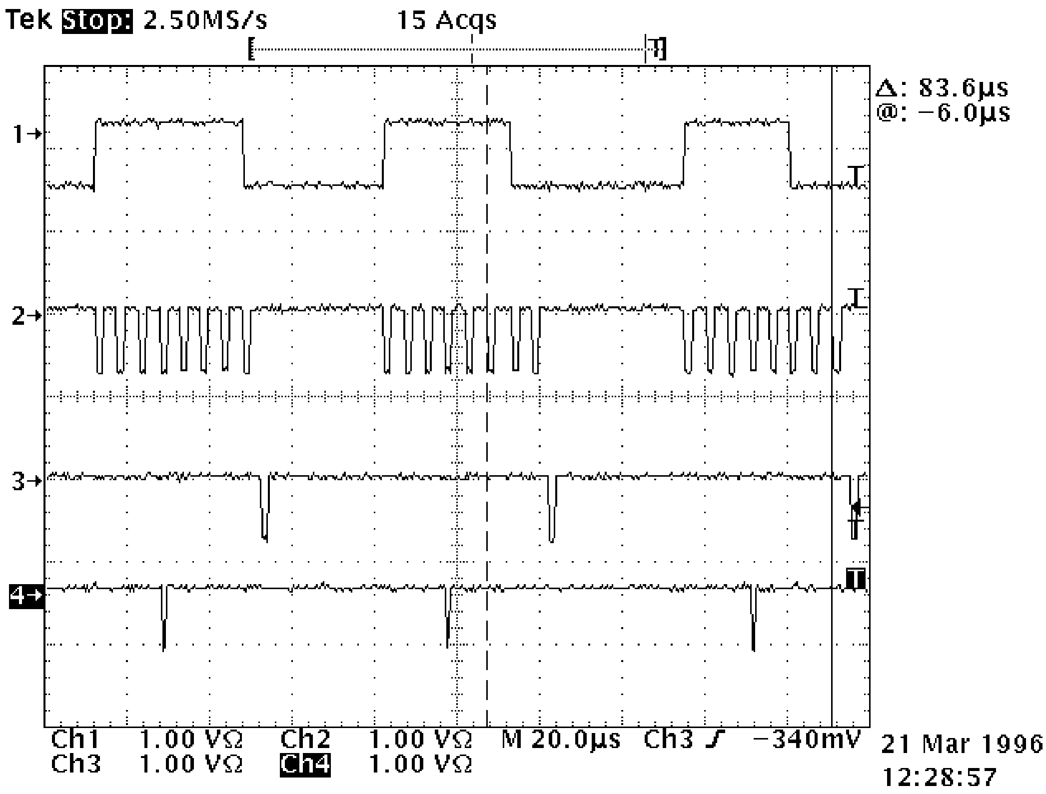

Figure 3.7.: FML write cycle for one byte (active low).
Channel 1: Data (1,3,7)
Channel 2: Clock
Channel 3: Load
Channel 4: irrelevant

3.11. 64 Digital Hit Multiplicity Flags for L3

In addition to the eight Trigger elements for the CTL1 and CTL2 and the 64 layer coincidence signals for the CTL2, the Central–μ–Detector also provides data to the (not yet operational) third level of the H1 trigger. The Read Out Controllers (ROCs) which collect the data from the pipelines in the WDMBs [31] [10] count the number of hits for all connected digital channels (wires and strips) and set a flag if a certain programmable hit threshold is exceeded. This information is collected by the cluster processors. The coordinating processor finally transmits them to the L3 memory [10]. The production of these 64 flags starts at L1K and takes about 500 μs (for the data of two bc). This is much too slow for L2 (compare section 2.2), so this data is available at L3 and later only.

4. Usage and Setups of the Electronics

4.1. Wire Digital Module Boards

The first parameter which influences the production of digital (trigger) signals on the WDMBs is the digitisation threshold voltage.
At the digitising comparator, the peak voltage of an average analog streamer signal in the LSTs is up to $\sim$ 200mV. Since in the synchronisation step of the signals their active length is of no importance (the first Flip Flop is gated with the signal itself), the threshold is determined by the noise level exclusively. The thresholds are set to 80mV which leads to high efficiency and low noise sensitivity.
The initial synchronisation to the experiment clock of the digitised signals is done on the WDMBs (section 3.1). For an efficient derivation of a trigger signal it is very important to receive the contributing signals originating from an e–p interaction always in the same bc w.r.t. the interaction bc t_0 . This is achievable by a careful adjustment of the phase of the synchronising HClk to the digital wire signal. The constraints by the detector hardware, electronics and their consequences for the trigger timing are discussed thoroughly in the next chapter.
Furthermore, as a fast trigger output, the 16fold instead of the double eightfold WOR is chosen. This loss in granularity has no consequences on the system efficiency, or any resolution since the trigger electronics is not able to detect and trigger on vertex pointing tracks in particular [1]. This is not the purpose of the trigger system, so this first step to reduce the trigger data is reasonable.

4.2. Layer Boards

A particle penetrating a module generates hits in most of the layers (according to the chamber efficiency of $\sim 83\%$). Thus the requirement of a certain minimum multiplicity of ELORs in a module represents a reasonable condition for the detection of a penetrating track, but without any information on its origin (the vertex).

4.2.1. Definition of five Iron Layers as Trigger Layers

Not all LST layers of the Central–μ–Detector contribute to the derivation of the TEs. There are several reasons for this. The layers inside and outside the iron (the μ-boxes,

[1] It only complicates the exclusion of single noisy wire signals from the trigger.

layers 0–2 and 13–15) are not used for the trigger since they are relatively sensitive on synchrotron radiation or back scattered beam products, i.e. the position of the collimators, which are intended to shield H1 from this. Only minimum ionising particles are expected to enter the interior of the iron. To achieve an early and sensible data reduction, without losing too much information, not all ten iron layers are connected, but the following five:

- layers 3, 4, and 5 are intended to detect lower energetic muons which do not pass all iron layers of the module due to their track curvature. Additionally, muons from pions showering in the first iron slab shall be observed (by layer 3 in particular, see below).
- layers 8 and 12 then serve to validate the passage of the entire module by the particle

With this decision, even for the strictest layer coincidence condition used, the trigger efficiency is about 80% [34].

4.2.2. Two Output Signals per LB (Layer Coincidence and t_0)

Two of the maximum eight output bits of the LB RAMs are used to produce the TEs. Bit 0 indicates the fulfilling of the multiple ELOR coincidence condition, bit 1 represents the activity of any of the ELOR signals required for the coincidence condition. Since the background conditions and rates in the 64 modules are very different, different coincidence conditions have been chosen:

1. Layer Coincidence conditions:
   a) Backward Endcap: hits in greater or equal three layers of the connected five (in short: $\geq$3 out of 5). This leads to minimal background rate from cosmic muons, since wire layers are perpendicular to the z– (beam) axis. For muons produced in ep–interactions, this condition is sufficiently strict to suppress triggers induced by hardware noise, but still leads to an efficiency above 95%. The modules directly around the beam pipe are suffering extremely from the proton beam halo. For this reason, for modules 8 and 9 a stricter condition to trigger exclusively module penetrating muons (tracks) was necessary: $\geq$2 out of $\{3,4,5\} \wedge \geq 1$ out of $\{8,12\}$.
   b) Barrel: $\geq$2 out of the inner four layers (3,4,5,8). Since in these modules the fraction of the trigger rate originating from particles from the vertex is relatively low ($\mathcal{O}$(Hz)), this soft(er) condition represents a lower p_T–threshold and leads to a higher efficiency. A minor disadvantage is the increasing sensitivity to chamber noise.
   c) In the forward region the (ep–collision) particle rates are much higher than in the Barrel or the backward region of the H1, so in order to improve the quality of the triggered muon events and to minimise the fraction of triggers by cosmic muons in the Forward Outer Endcap $\geq$3 out of $\{3,4,5,8,12\}$ is required. Analog to modules 8 and 9 in the Backward Endcap, for the entire Forward Inner Endcap a condition $\geq$4 out of $\{3,4,5,8,12\}$ is chosen, due to the boosted collision products in direction of the proton.

2. t_0 information from the condition 1 out of the n layers considered in the coincidence condition: The LSTs and –elements are staggered w.r.t. tracks perpendicular to the layers (see figure 1.7). Thus it is allowed to assume that at least one of the streamer signals from the layers considered in the coincidence condition reaches the synchronisation electronics on the WDMB always in the same and correct bc. The layer coincidence signal (if observed at all) then either is detected in the same bc or one bc later. In the first case, due to the signal elongation on the LBs, it is at least two bc long, otherwise it is of course at least one bc long. Details on this matter are discussed comprehensively in chapter 5.
   This additional signal per module has been used since 1995.

4.2.3. The Element Majority Logic for Layers 3

The signals indicating that more than one (respectively two) element(s) of layer 3 were hit (compare figure 3.4), which are foreseen to veto shower muon events, are not used. On the one hand the overall fraction of rejectable events and therefore the possible reduction of the trigger rate is negligible, on the other hand the criterium of more than one hit element is too weak to detect showers. It is too likely to reject triggers from events with two tracks in the respective module.
Figure 4.1a shows for each module the fraction of events in which more than 1 element in layer 3 was hit in those for which a layer coincidence was detected. Only in the inner Endcaps this fraction is about 5% or larger, especially for the two modules around the beam pipe (8, 9 respectively 56, 57).
Figure 4.1b shows the mean number of digital hits (incl. strips) for these events again for each module separately. For the inner Endcap modules the mean number of digital hits is about 20 which is approximately the expected number of hits for two tracks.
Finally figure 4.1c shows the distributions for the numbers of hits per module if exactly 1, 2, or 3 elements in layer 3 had been hit.

4.3. Sector Boards

4.3.1. Parallel Processing of Layer Coincidence and t_0 Signals in two Sector Boards

The t_0 and the coincidence signals are intended to be joined to a signal with both the information on the fulfilled layer coincidence condition and the correct t_0 bc. Although this could be done on the MPSDCs, this step of signal processing is delayed up to the GPTP Board, because its monitor pipelines of the inputs allow a further separate analysis of the signals offline. So the 128 signals which had been delayed on the H1MPSDCs are processed separately w.r.t. their meaning in two SBs, whose RAM LUTs are set up identically. SB0 processes the 64 layer coincidence signals, SB1 the 64 respective module–t_0–signals.

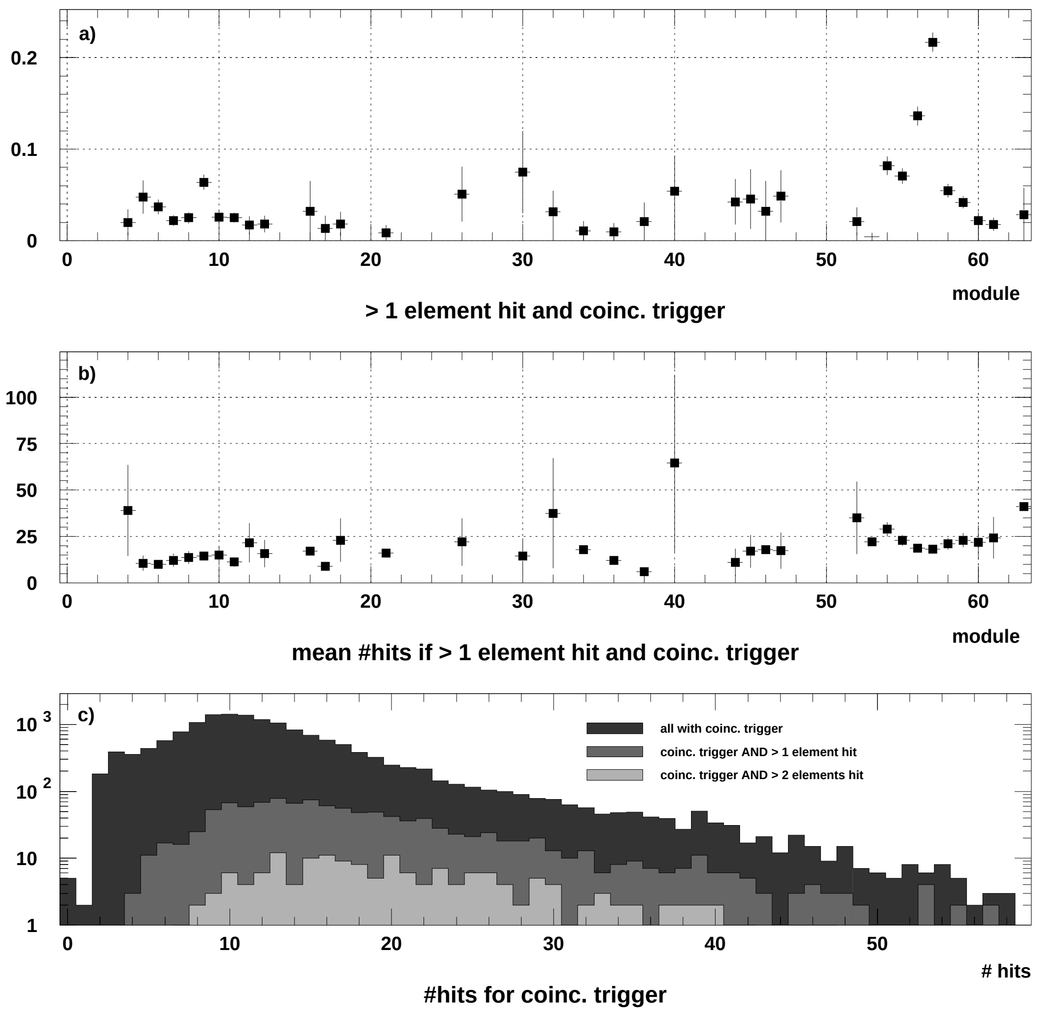

Figure 4.1.: a) Fraction of events with more than 1 element hit if layer coincidence condition fulfilled b) mean number of hits for events in a) c) number of hits for the number of hit elements > 0, > 1, > 2

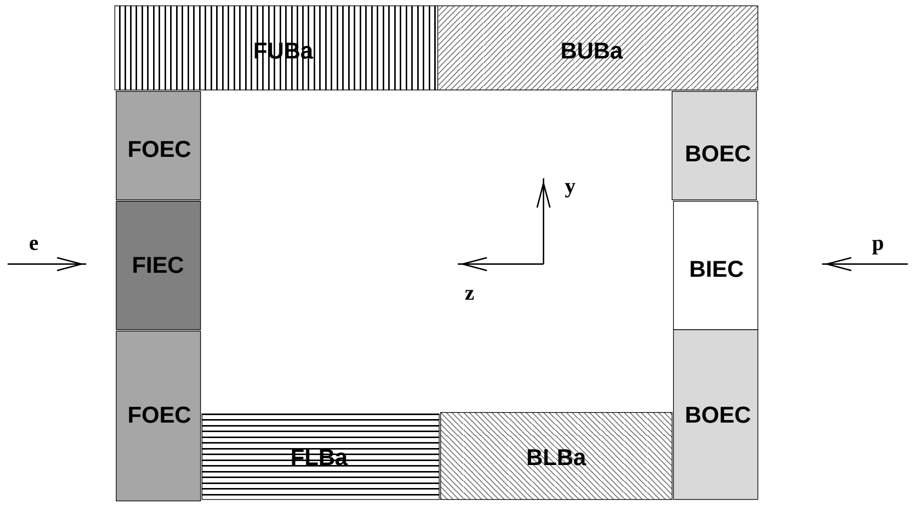

Figure 4.2.: Definition of trigger sectors by the Sector Board

4.3.2. The Division of the Detector into Trigger Sectors

In order to reduce the number of signals to 32 (the number of GPTP inputs), the first of the two SB features mentioned in section 3.6 is chosen: consecutive modules are unified to eight trigger sectors. As a consequence the granularity is decreased. This is done with consideration of not only the intended final meaning of the TEs, but also the opportunity to analyse calibration data and to monitor the system performance in general. So each SB provides 16 output signals to succeeding level of processing: the outputs of SB0 contain the information on the multiplicity of layer coincidences greater 0 and greater 1 for each defined sector. SB1 provides the respective sector–t_0–signals. The assignment of modules to the trigger sectors is defined in table 4.3.2 and visualised in figure 4.2.

Location	Abbreviation	modules
Backward Outer Endcap	BOEC	(0–5)+(12–15)
Backward Inner Endcap	BIEC	6–11
Backward Upper Barrel	BUBA	16–24
Backward Lower Barrel	BLBA	25–31
Forward Upper Barrel	FUBA	32–40
Forward Lower Barrel	FLBA	41–47
Forward Outer Endcap	FOEC	(48–53)+(60–63)
Forward Inner Endcap	FIEC	54–59

Table 4.1.: Assignment of modules to trigger sectors

4.3.3. Combination of Information from different μ–Subdetectors

The alternative SB feature to reduce the amount of data is the ORing of the signals from two adjacent modules. It allows the combination of the information from two different

μ–subdetectors in one SB LUT RAMs. This feature remains unused since at this level there would be a too early loss of valuable information. The created ambiguities become very uncomfortable, for example when combining the data from the Backward and Forward Endcap with the intention to detect beam halo muons, because the information on the (raw) x coordinate is completely lost. In addition the ambiguities should be minimised before the data transmission to the GPTP, for monitoring purposes.

4.4. GPTP

4.4.1. Combination of the t_0 and Coincidence Information to the Trigger Elements

Up to 1995 only one output bit per LB was used which indicated the fulfilling of the multiple layer coincidence condition. An accelerated read out hardware and software allowed the read out of the digital data of four single bc (bc -1 to 2) within the time window required by the CDAQ (1995: 1.2 ms) [10]. [2] Therefore with a respective trigger simulation package, a timeslice wise trigger verification was possible and so a much better monitoring of the trigger and read out.
Due to large drift times and the therefore necessary signal elongation on the LBs, the coincidence signals often are longer than one bc or reach the CTL1 one bc too late. So the muon trigger information could only serve to validate other trigger conditions but not to provide any precise information on the t_0 since the information, when trigger element was (first) active was distributed over $\geq$ 2bc.
Figure 4.3 shows this distribution for muon events triggered in a standard luminosity run and the respective distribution of the event t_0 reconstructed from tracks in the CJC. With the assumption made for the timing of the module–t_0–signal (4.2.2) it is possible with the following logic, to achieve the two goals both to receive the trigger element signal in the correct bc and to reduce its length to one single bc:

The module–t_0–signal indicating whether one of the trigger layers at all detected a hit, is delayed by one bc w.r.t. the signal indicating the fulfilling of the layer coincidence condition. After this relative delay, the two signals are logically multiplied at each bc (AND mode of GPTP Board, see 3.8) and the result is transmitted to the CTL1 as the respective trigger element. The resulting trigger element has a length of one bc and the correct timing i.e. it is active exclusively in bc 0, independent if the initial layer coincidence signal was active coincidently with the t_0-signal or one bc later. Figure 4.4 shows this manipulation of the trigger signals for the case, that in two trigger layers a hit had been detected.
The result is a much sharper, more reliable t_0 information from the Central–μ–Trigger and a decreased background rate due to random coincidences.

[2] Before 1995, the information in a time window of two bc was read out, and for each single wire pipeline, two succeeding bc were logically added. This necessitated only one read out cycle and fulfilled the velocity criterium of the CDAQ (in detail in [31] [10]).

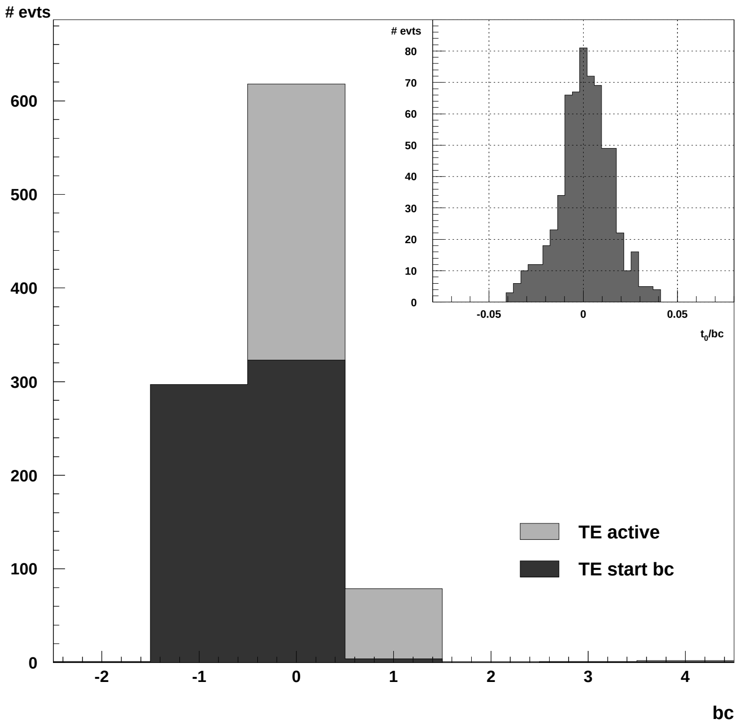

Figure 4.3.: Exclusive usage of the coincidence signal for the TE: Distributions of all and first timeslices in which TE was active (TE Mu_BIEC>0, for a layer coincidences in only one module of the sector, luminosity run 181249). The insert shows the distribution of the t_0 reconstructed from CJC data.

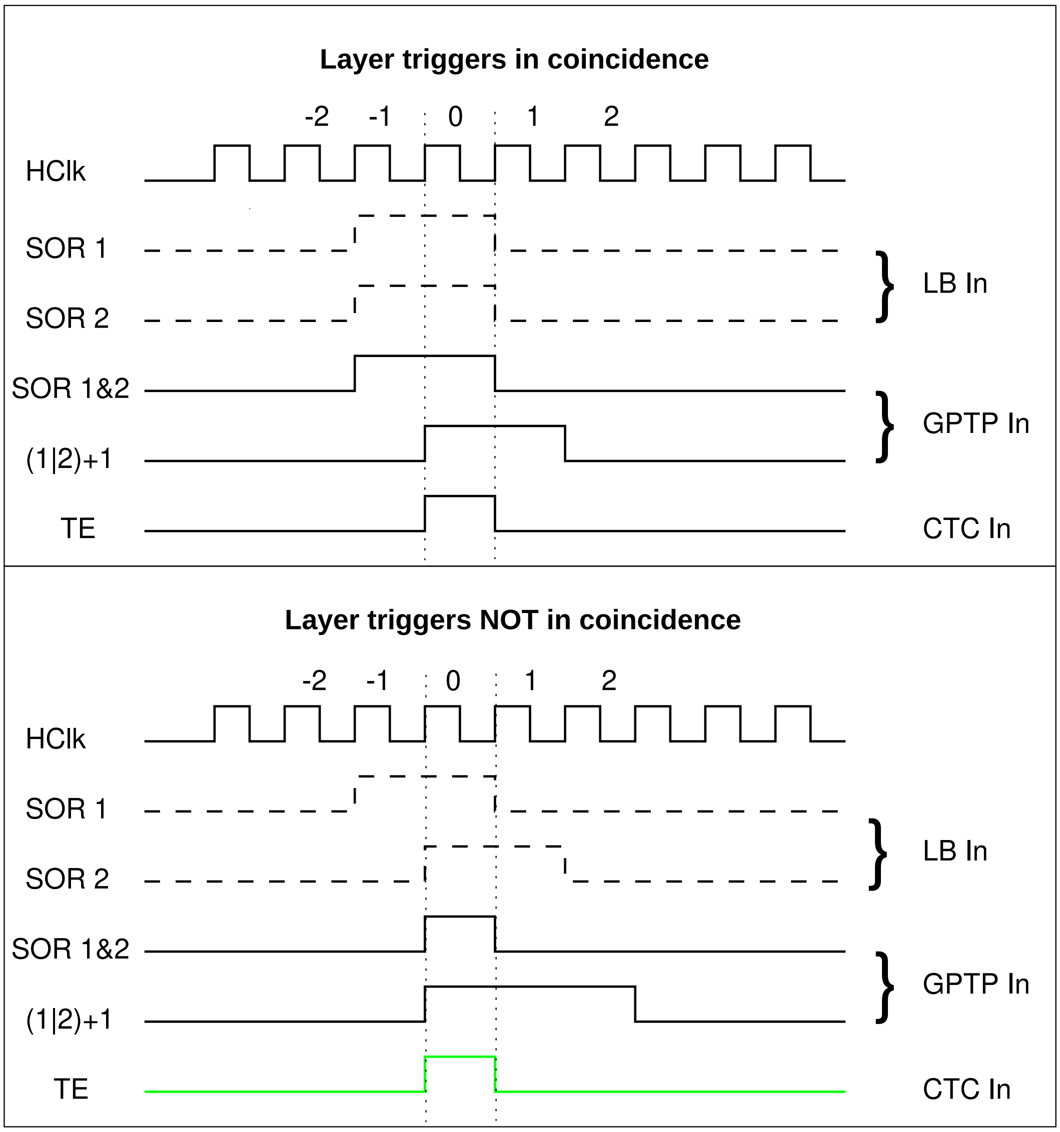

Figure 4.4.: Combination of the sector coincidence and t_0 signal to the final μ–TE.

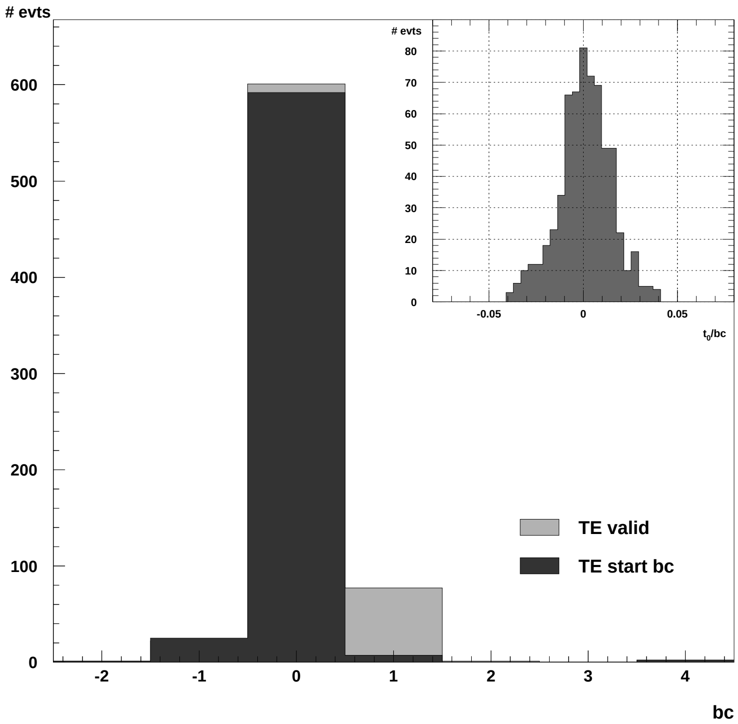

Figure 4.5.: Usage of the coincidence and the t_0 signal for the TE: Distributions of all and first timeslices in which TE was active (TE BIEC>0, for a layer coincidences in only one module of the sector Luminosity run 181249). The insert shows the distribution of the t_0 reconstructed from CJC data.

4.4.2. Division of the Detector into five ϑ Trigger Sectors

Since it is/was not possible to install a fast track trigger for the Central–μ–Detector , the Central–μ–Trigger 's aim is to trigger certain event topologies in the H1 detector. So in another step of data reduction, the eight trigger sectors defined in the SB are combined to five final TE sectors in ϑ. The interesting value in high Q^2 e-p events is the ϑ of the muon track. This suggests to divide the Central–μ–Detector in ϑ–sectors for trigger purposes, too, although especially in the Barrel region this information can be only vague, due to the wire orientation parallel to the z–axis. Since the most detector activity is observed in the Endcaps (esp. the FEC) the Central–μ–Detector was divided into two ϑ–sectors with three trigger conditions each in either Endcap and one sector with two trigger conditions for the entire Barrel region. The sectors of the resulting Trigger Elements, their names and the considered input signals shows the following table 4.2 [3].

sector	TE name	condition on inputs from SB
Backward Inner Endcap	Mu_BIEC	BIEC>0
Backward Outer Endcap	Mu_BOEC	BOEC>0
Backward Endcap	Mu_2_BIoOEC	BIEC>1 OR BOEC>1
Barrel	Mu_Bar	(BUBA+BLBA+FUBA+FLBA)>0
Barrel	Mu_2_Bar	(BUBA+BLBA+FUBA+FLBA)>1
Forward Inner Endcap	Mu_FIEC	FIEC>0
Forward Outer Endcap	Mu_FOEC	FOEC>0
Forward Endcap	Mu_2_FIoOEC	FIEC>1 OR FOEC>1

Table 4.2.: The TEs of the Central–μ–Detector and their meaning

The respective coverage of the ϑ–φ–plane by the sectors can be derived from figure 1.6. The eight TEs then are transmitted successively for each bc to the CTL1.

[3] Due to the octagonal cross section of the iron yoke its geometry is more cartesian rather than cylindrical, so the ϑ–sectors still depend on φ.

5. The Trigger Timing and its Calibration

The basic aim of any L1 trigger subsystem is the creation of the TEs in the t_0 bc if a particle from an interaction at the vertex passed the respective subdetector.
Since the t_0 bc is defined by the L1ASTs, the correct timing of the H1 TEs is particularly important for the rates of physics L1ASTs which combine the information from several subdetectors. In a large detector as the Central–μ–Detector with the logics applied in its trigger system, TEs of length one bc are produced, which can originate from signals in about 30,000 LSTs. So, the condition for an efficient trigger, to synchronise all possible source trigger signals in a way that the final TEs arrive at the CTL1 in the correct bc 0, is not trivial. The timing of the Central–μ–Trigger depends on many characteristic values of the H1 detector, the LST chambers, and the design of electronics. To understand the constraints in optimising the Central–μ–Trigger timing, the most important items are explained, before the trigger timing is simulated and the calibration itself is presented.

5.1. Conditions and Constraints for an Accurate Trigger Timing

The time from the muons' production in the interaction region and their earliest possible detection in the WDMBs of the trigger layers be called detection time t_{det}.
It is determined by the sum

$$t_{\text{det}} = t_0 + t_{\text{flight}} + t_{\text{drift}} + t_{\text{trans}} \tag{5.1}$$

With

- t_0 , the (reconstructed) interaction time relative to $t = 0$ which is defined by the respective L1AST
- t_{flight} , the time of flight of the muon from the interaction region into one of the trigger layers of a Central–μ–Detector module
- t_{drift} , the drift time between the passage of the LST by the muon and the arrival of the produced streamer charge on the wire
- t_{trans} , the transmission time of the initial streamer signal from its arrival on the wire to the change of the output state of the first flip flop in the pipeline on the WDMB (figure 3.3)

The width of the $t_{\rm det}$ spectrum has to be lower than 96ns in order to guarantee a unique assignment of the signals to a specific bc. In this context the minimum value of $t_{\rm det}$ itself is completely irrelevant. Presuming that the signal elongation on the LBs (section 3.3) to a length of two bc guarantees the detection of layer coincidences, for a correct timing equalisation to the t_0-signals (section 4.4.1) the condition on $\sigma(t_{\rm det})$ [1] ,the width of $t_{\rm det}$, is focused on the hit i with the minimum $t_{\rm det}$ of all N hits contributing to the layer coincidence:

$$t_{\rm det} = min(t_{\rm det.,1}, ..., t_{\rm det.,N}) \tag{5.2}$$

To visualise the relation between the width of the $t_{\rm det}$ distribution and the possibility to synchronise the respective signals in a way they are assigned to to the same bc, assume a detection time $t_{\rm det}$ uniformly distributed with $p_{\rm det}(t_{\rm det})$ and a width $\sigma(t_{\rm det}) = 75$ns for $t_0 = const. = 0$ as shown in figure 5.1a. Since in luminosity data, the t_0 is reconstructed at $t_0 = 0$ with a very high accuracy, in the following, $\sigma_0(t_{\rm det})$ is defined as

$$\sigma_0(t_{\rm det}) = \sigma(t_{\rm det}(t_0 = 0)) = \sigma(t_{\rm det} - t_0) \tag{5.3}$$

The trigger signals becoming active (output of first flip flop on WDMB) at these times, shall be synchronised at different phases $t_{\rm synch}$ of the HClk w.r.t. t_0 (a:20ns, b:40ns, c:60ns, d:80ns). This is equivalent to different delays of the HClk provided to WDMBs and LBs by the CTC.
In this example, all other relevant signal phases in the system (such as the phase of the resynchronising HClk on the MPSDCs w.r.t. the LB output signal and the phase of the PEn w.r.t. the HClk driving the pipelines) may stay constant for all $t_{\rm synch}$. Consequently, the relevant edge of the synchronising HClk, insinuated by the lines at positions b)-e), determines the observation of the wire signals in bc n.
Figures 5.1b-e show the resulting distributions of bc in which the trigger signals were recognised to be active. In the latter gedanken experiment, figure 5.1e illustrates the achieved goal, to detect all trigger signals from muons produced at $t_0 = 0$ in the same bc. For $\sigma_0(t_{\rm det}) > 1$bc (neglecting further electronical restriction by edge slopes, etc.) , the triggers are observed in at least two succeeding bc. In the following the terms contributing to $t_{\rm det}$ have to be investigated more detailed, before a prediction concerning the fulfilling of the necessary condition can be made.

5.1.1. The Flight and the Transmission Times $t_{\rm flight}$ and $t_{\rm trans}$

The times of flight of a muon from the interaction region into a potentially triggering module are different (apart from energy dependent differences)

a) for different points within the same LST

b) for different LSTs within the same trigger layer

c) for the five trigger layers within the same module

[1] In the following for a rectangular distributed variable x, $\sigma(x)$ means the full width of the rectangle. Therefore $\sigma(x) = \sqrt{12} \int_{x_{min}}^{x_{max}} dx(x - \langle x \rangle)^2$

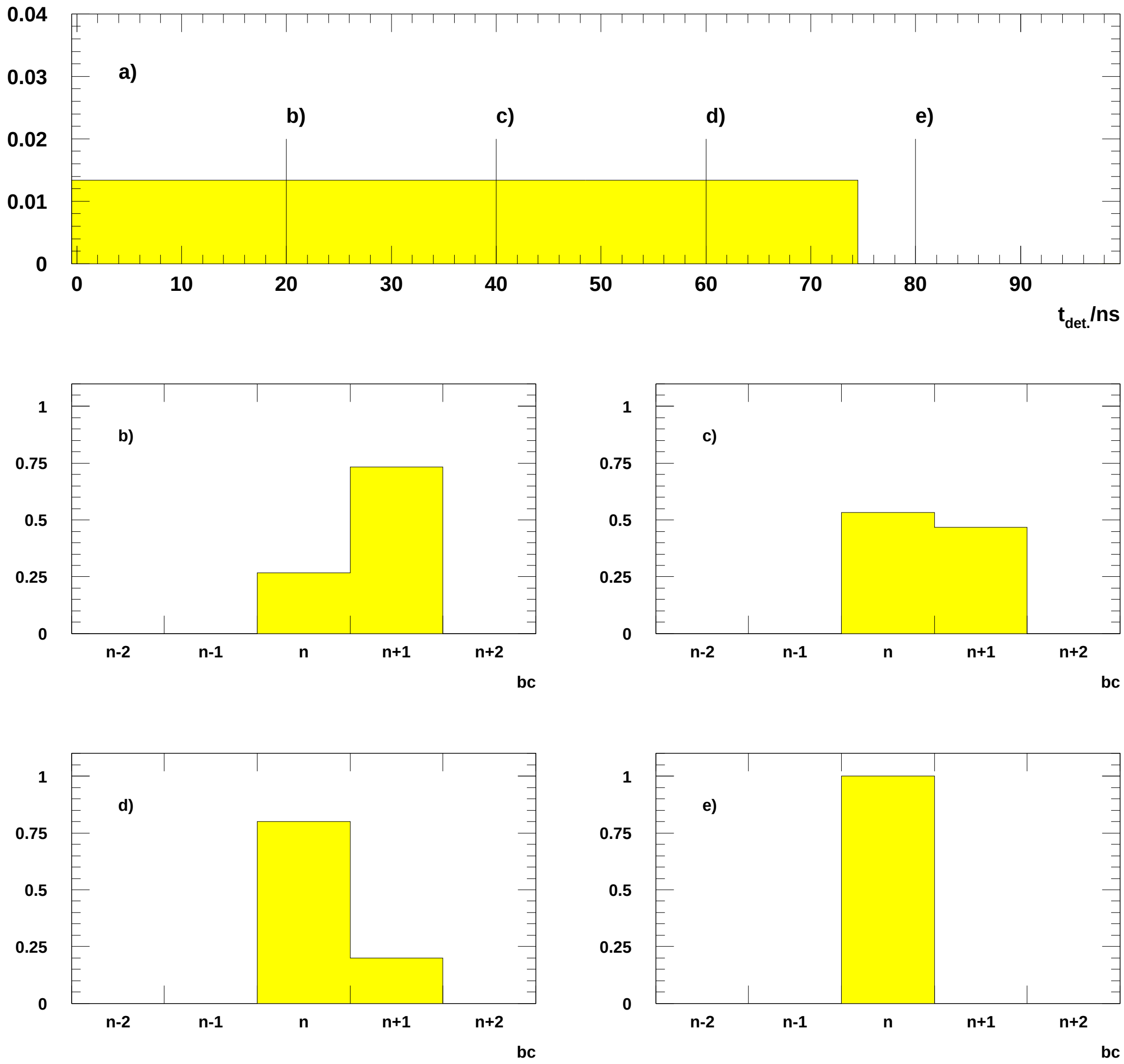

Figure 5.1.: Synchronisation of the initial digital wire signals
a) Normalised uniform distribution $p_{\mathrm{det}}(t_{\mathrm{det}}(t_0 = 0))$ of the detection time t_{det} of width 75ns
b)-e) Timeslice distributions resulting from different t_{synch} indicated in a)

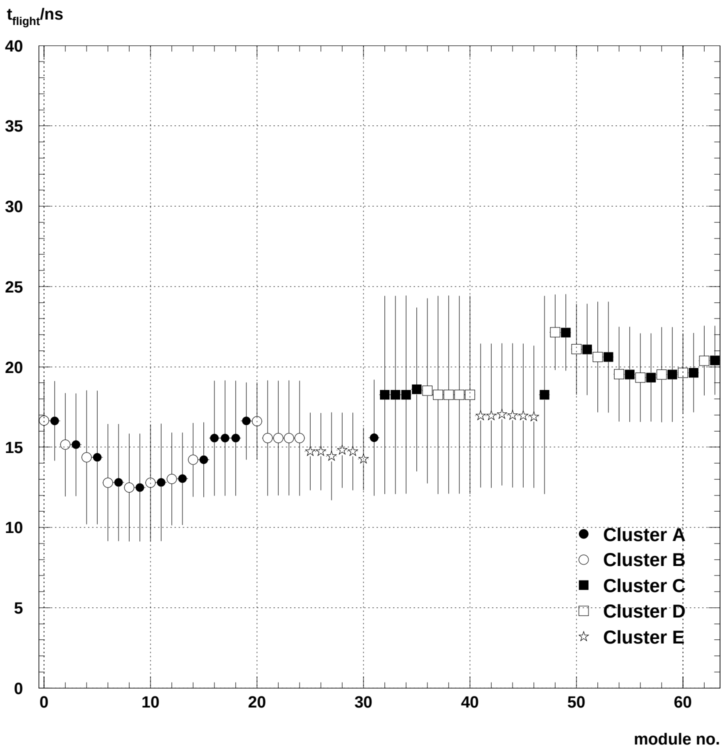

Figure 5.2.: Times of Flight t_{flight} for each module (trigger layers only)

d) for the 12 respectively 13 modules which are assigned to the same hardware cluster.

This is more or less inevitable, since the Central–μ–Detector cannot be a sphere around the interaction region.

In the following only high energetic muons with a very low curvature track are considered, for which t_{flight} is approximated by the distance R of the hit in the trigger layer to the nominal interaction point $(x = y = z = 0)$ [2]. This means for t_{flight}:

$$t_{\mathrm{flight}} = \frac{R}{c} \quad \text{with} \quad R = \sqrt{x_{\mathrm{hit}}^2 + y_{\mathrm{hit}}^2 + z_{\mathrm{hit}}^2}$$

The geometrical position of all LSTs and strips is stored in the H1 database. The coordinate in direction of the wire is derivable from the hit strips. Due to the size of the Central–μ–Detector (length in $z \approx 9.3\ m$, average Barrel radius $\approx 3.5\ m$) at wire lengths of up to 5.5 m, even if restricting to high energetic muons, the contribution of $\sigma(t_{\mathrm{flight}})$ to $\sigma(t_{\mathrm{det}})$ is not negligible. Figure 5.2 shows the range of these different times of flight from the vertex for each module. The error bars here do *not* indicate the uncertainty of the mean value at the marker's position, but the possible interval for t_{flight} for each module. An additional contribution to t_{det} originates from the transmission time of the signal on the wire to the WDMB. The WDMBs are installed at the end of the LST elements. This

[2] The length of a muon trajectory from the interaction region to the Central–μ–Detector (at all) depends on their velocity and the angle of their trajectory w.r.t. the magnetic field.

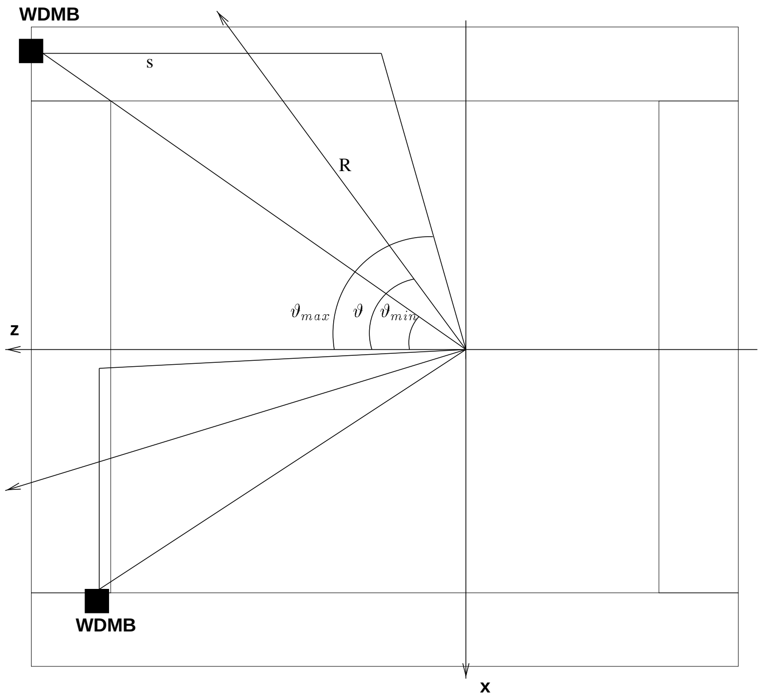

Figure 5.3.: The correlation of the time of flight t_{flight} and the transmission time t_{trans} (top view of the Central–μ–Detector).

is for all LSTs that end of the chamber with the maximum distance to the interaction region. So the time of flight t_{flight} and the transmission time t_{trans} are not uncorrelated: for large t_{flight}, t_{trans} is small and vice versa. By means of figure 5.3 one derives:

$$\frac{t_{\text{flight}} + t_{\text{trans}}}{t_{\text{flight, max}}} = \frac{1}{c}\frac{\sin\vartheta_m}{\sin\vartheta} + \frac{1}{c_{\text{wire}}}(\cos\vartheta_m - \sin\vartheta_m \cot\vartheta)$$

where

$$t_{\text{flight, max}} = t_{\text{flight}}(\vartheta_m)$$

and $\vartheta_m = \vartheta_{min}$ for the BEC and the FBa and $\vartheta_m = \vartheta_{max}$ for the BBa and the FEC respectively. In comparison to the assumption that the muon moves at the speed of light, the signal velocity on the wires is considered by $c_{\text{wire}} \approx (5\text{ns}/m)^{-1} = 20\text{cm/ns}$. As a consequence, the value remaining relevant for the width of t_{det} and therefore for the possibility to synchronise the entire t_{det} spectrum, is the range of the sum $(t_{\text{flight}} + t_{\text{trans}})$ since its width increases the width of t_{det}. They are depicted in figure 5.4 for each module of the Central–μ–Detector separately. The sum of flight and transmission time $t_{\text{flight}}+t_{\text{trans}}$ for all detector modules

5.1.2. Drift Time Distribution

The main contribution to the width of t_{det} originates from the width of the distribution of the drift time distribution, the time it takes the streamer in the LST gas volume to reach the wire.

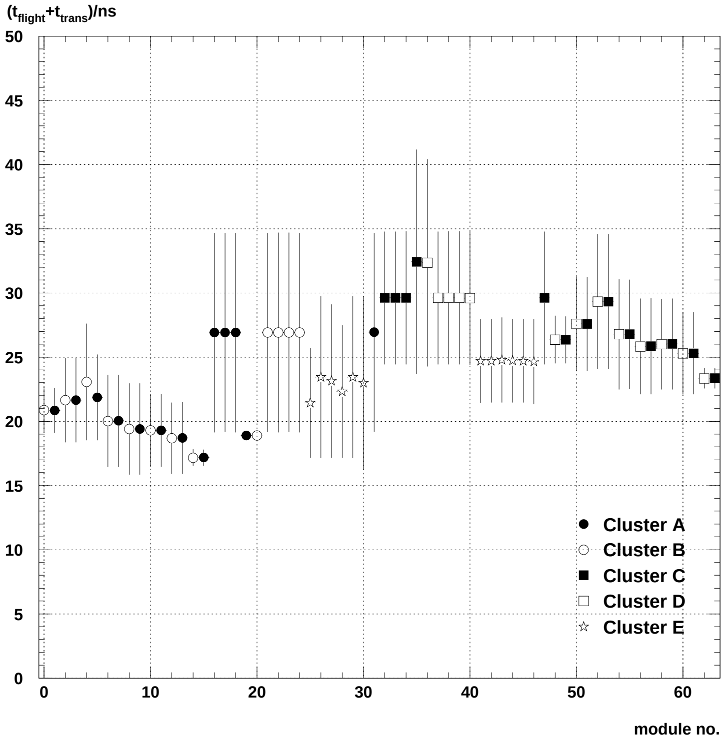

Figure 5.4.: The sum of flight and transmission time $t_{\text{flight}} + t_{\text{trans}}$ for all detector modules

As already mentioned in section 4.4.1 and shown in figure 5.5, the drift times in the LSTs of the Central–μ–Detector range from a minimum near zero up to about 140 ns which is definitely greater than one bc (96 ns). The *length* of the initial wire signal is irrelevant since the first flip flop is gated by the edge of the digitised wire signal itself and not by the HClk (compare figure 3.3). The probability that the drift time is greater than 75 ns is 11% and the probability, that it is greater than 96 ns is about 4%. The drift time is mainly determined by the distance of the muon's trajectory to the wire. For an active TE from the Central–μ–Detector , trigger signals from at least two trigger layers are required (compare section 4.2). Presuming that streamers are produced in (at least) two trigger layers and that the drift times in these layers are independent the drift time in at least one of the LSTs is below 75 ns with a probability of greater 98%, In addition to the contributions of t_{flight} and t_{trans} and at a constant interaction time t_0, which is the case in standard luminosity running, this fulfils the condition $\sigma_0(t_{\text{det}}) < 96$ns for all modules separately.

5.1.3. Distribution and Delays of the HClk and the Trigger Signals

In addition to the fact that it is not guaranteed, that for each event the minimum t_{det} of the hits in the trigger layers of the respective modules is lower than 96 ns, the important phase t_{synch} of the synchronising HClk w.r.t. the digital wire signal on the WDMBs (for $t_0 = const$) is not adjustable for each individual WDMB and not even module wise. Figure 5.6 shows the distribution of the HClk to the L1 trigger electronics, the flow of

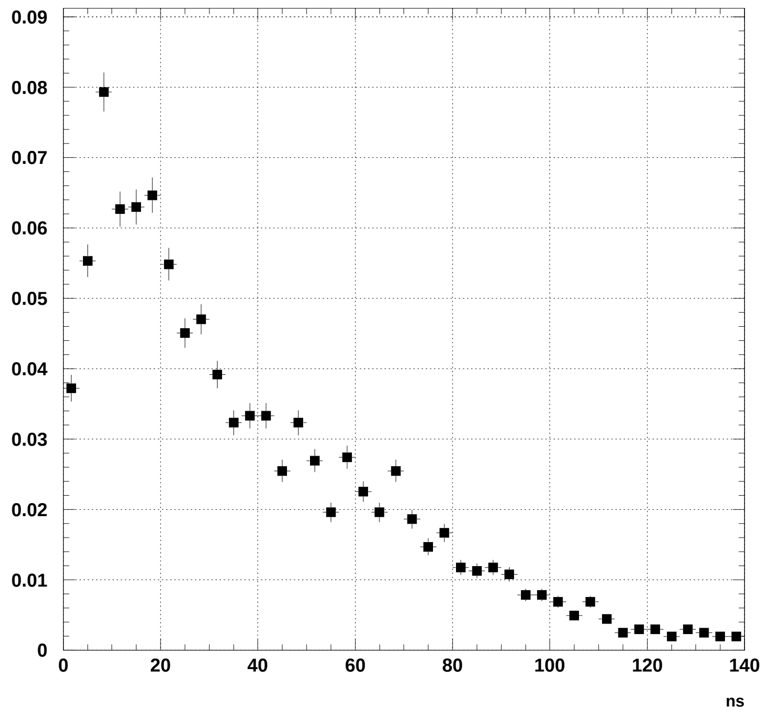

Figure 5.5.: Normalised drift time distribution $p_{\mathrm{drift}}(t_{\mathrm{drift}})$ in an LST, with the three–component gas and a high voltage of 4.5kV without a magnetic field (from [35])

the trigger signals, and the possible delays of these signals on the individual devices (step size/maximum delay in bc).

The HClk signal together with the signals RUN, PEn, L1Active, and FsClr is delivered to the subsystem trigger controller crates (STC) by the Central Trigger Controller (CTC). Special Fan Out Cards (FO) distribute the signals to the ROC– and LB–crates of the five hardware clusters on the detector galleries, on top of H1. They allow a shift of the active edge of all signals within a time window of one bc and provide them in RS422A differential standard via twisted pair flat cable (of length l_X), to minimise the influence of external electronic noise. [3] The features of the Read Out Controllers themselves do not permit the realisation of any (HClk) signal delay for each module individually (see [10]). On the Clock Receiver Cards in the LB crates, the HClk can be delayed in steps of a quarter of a bc, to adjust its phase to the LB input signals according to the experiment standard of signal validity 20 ns before the active edge of the synchronising/validating HClk. With this delay set once, the phase of the fast WDMB trigger output signal to the resynchronising HClk on the LB is constant, independent of the HClk delay on the Fan Out Card.
The possibility to realise any (HClk) signal delay for each module individually exists neither on the Read Out Controllers nor on the LBs. The design of the signal distribution

[3]The HClk signal can be delayed in steps of 1.5ns = bc/64 ,
the PEn signal can be delayed in steps of 6ns = bc/16.

hardware does not even allow a separate influence on the time behaviour of read out and trigger branch separately.
So, the time behaviour can be influenced in the way described in the previous section only cluster wise via the HClk delay on the Fan Out Cards. This means, the relevant width of t_{det} is determined by the minimum and maximum detection times *in each cluster*. The problem with this lack in degrees of freedom in the system is also discussed in [10].
The delay of the LB output signals (section 3.3) is foreseen to equalise the different cable lengths l_{Cluster} (maximum 30m $\approx$ 150ns) from the cluster crates to the Patch Panel in the electronics trailer. For an additional correction of the timing in steps of an integer number of bc, the delay range of 2.75 bc often is insufficient. So, before the installation of the H1MPSDCs, the LB output signals did not arrive at the SB with the same phase to the HClk. The HClk which resynchronises the output of the SB LUT RAMs is adjustable only in steps of a quarter of a bc on the Clock Receiver Card in SB crate.
In the latter construction, the recognition of module coincidences was not guaranteed since the length of the respective output signal of the SB LUT RAM was only lower or equal to one bc. So with the installation of the H1MPSDCs in their default setup, resynchronising and delaying the trigger signals by an integer number of bc, the latter two inadequacies in the design of the data flow were redressed:

- The additional resynchronisation of the trigger signals before the SB LUT RAMs increases the efficiency of the two-μ-TEs (Mu_2_BIoOEC, Mu_2_Bar, Mu_2_FIoOEC). The phase of this resynchronising local HClk derivate w.r.t. to the official HClk in the CTL1 (which defines $t_0 = 0$) in following will be called t_{resynch}
- The possible signal shift by an integer number of bc at least allows tuning the trigger timing in units of bc. This supplementary delay of the signals in the following will be called t_{MPSDC}

5.1.4. Constraint by the Read Out Timing

The acceleration of the Central–μ–Detector read out in 1995 allowed the read out of the digital data of four single bc (bc -1 to 2) within the time window required by the CDAQ [4]. Hereby it was possible and for the first time reasonable, to determine a mean track–t_0 from the time information of all wire and strip hits assigned to a certain track [36]. Since this track–t_0 is intended to give information on the *mean* time of detection, it is calculated for a track i with N wire hits which were first detected in bunch crossings $t_{1,\dots,N}$ as

$$t_{0,i} = \frac{\sum_{k=1}^{N} t_{i,k}}{N} \tag{5.4}$$

The track–t_0 is monitored during the data acquisition on L4. By means of the four–bc read out, a resolution $\sigma(t_0) \approx 20$ns is achieved. This implies that the synchronising edge of the HClk on the WDMBs at the optimal position for the read out should be at the mean t_{det}. That would mean for the trigger timing a lower probability to detect at least one of the hits in the trigger layers in the earliest possible bc (compare to beginning of this

[4]Before 1995, the information in two bc was read out, but for each single wire pipeline, the two succeeding bc were logically added. This necessitated only one read out cycle (in detail in [10]).

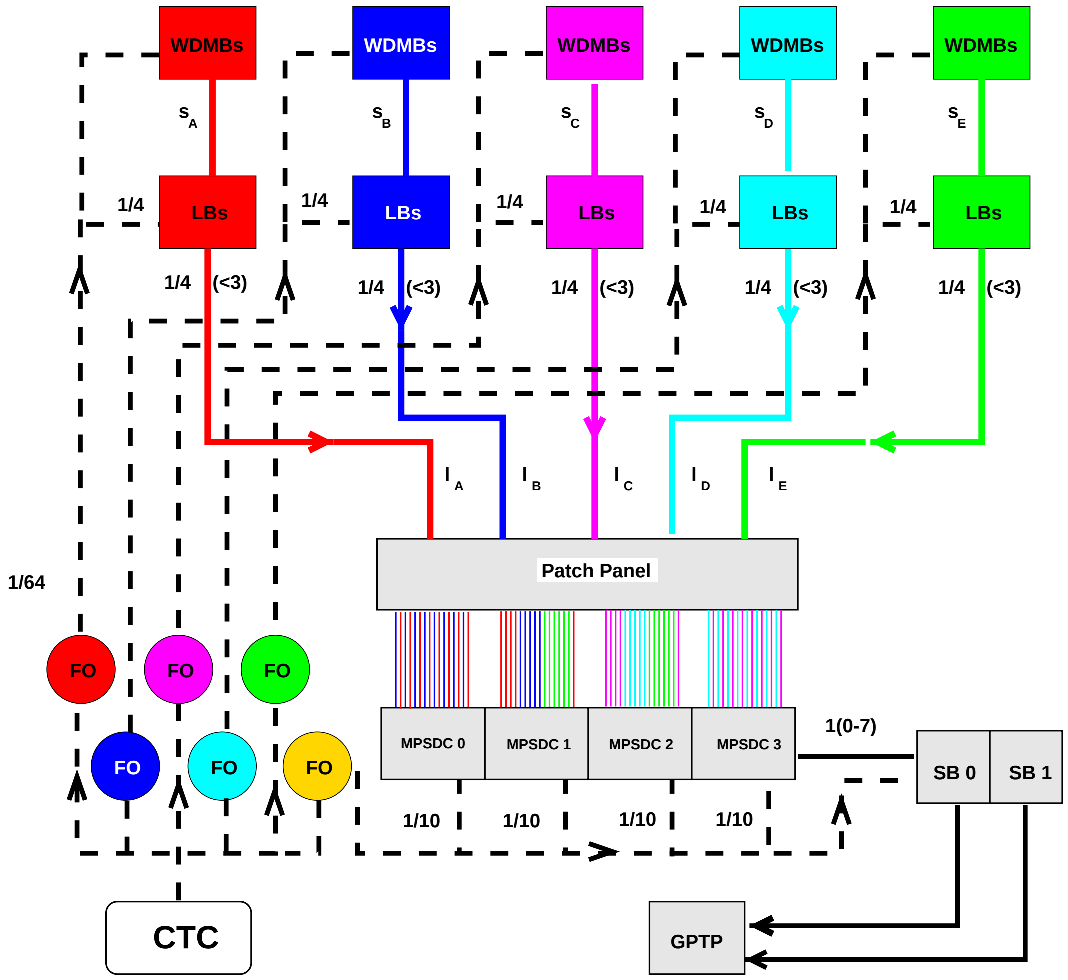

Figure 5.6.: The distribution of the HClk to the Central–μ–Trigger System from the CTC to the WDMBs and the data flow back to the GPTP. Expressions like 1/n(<m) indicate the possibility to delay the respective signal in steps of $\frac{1}{n}$ bc in a range up to m bc

section). In addition, the read out and the trigger data are stored in different pipelines, driven by HClk derivates with different phases w.r.t. t_0. Due to these different goals and the mentioned lack of degrees of freedom in the system setup, a compromise has to be found in the calibration (see section 5.3).

5.2. Simulation of the Trigger Timing

For a realistic simulation of the trigger timing, which has been depicted over simplified in figure 5.1, in addition to t_{det} and t_{synch}, the following parameters have to be considered for the determination of the bc bc_{trig} in which the TE will be observed:

- t_{resynch}, the phase of the resynchronising HClk on the H1MPSDCs w.r.t. the LB output signal
- t_{MPSDC}, the modulewise adjustable delay on the H1MPSDCs (in steps of 1 bc)
- t_{GPTP}, the length of the delay pipeline on the GPTP

Mathematically, bc_{trig} can be expressed as follows (all times in units of bc): [5]

$$\begin{aligned} bc_{\text{trig}}(t_{\text{det}}) &= \text{ceil}(t_{\text{det}} - (t_{\text{synch}} \text{ modulo } 1)) \\ &\quad + \Theta\left[(t_{\text{synch}} \text{ modulo } 1) - (t_{\text{resynch}} \text{ modulo } 1)\right] + t_{\text{MPSDC}} + t_{\text{GPTP}} \end{aligned} \tag{5.5}$$

In this notation, for $t_{\text{MPSDC}} + t_{\text{GPTP}} = 0$ and $t_{\text{synch}} < t_{\text{resynch}}$, t_{synch} defines the assignment of the trigger to bc 0. Both t_{synch} and t_{resynch} are smeared by unequal cable lengths: t_{synch} by unequal lengths s_{cluster} of the cables transmitting the trigger signals from the WDMB to the LB (compare figure 5.6), t_{resynch} by clusterwise different cable lengths $l_{clusters}$ from the LBs down into the H1 electronics trailer, to the H1MPSDC input ports. Due to this, t_{synch} is not equal for all modules assigned to the same hardware cluster, and it cannot be achieved that for all t_{det} the signals are assigned to the same bc. If the LB output delay and the phase of the resynchronising HClk w.r.t. t_0 are kept constant, for $t_{\text{synch}} > t_{\text{resynch}}$, the synchronised LB output signals are validated on the MPSDC by one HClk edge later than for $t_{\text{synch}} < t_{\text{resynch}}$ and so are assigned to the succeeding bc. This is due to the fact that the HClk driving the GPTP pipeline has a constant phase to PEn. So, the decision on the bc in which the trigger signal will be observed is already taken one (re)synchronisation step earlier.
If due to the contribution of the term $\Theta(t_{\text{synch}}\text{modulo}1 - t_{\text{resynch}}\text{modulo}1)$ the final bc is not equal 0, this can be equalised by t_{MPSDC} modulewise, or, in case of a global offset of all TEs, by an adequate change of t_{GPTP}.
To obtain a more precise measurement of the dependence of bc_{trig} on t_{det}, and first of all the dependence on t_0, one has to give up the constance of t_0. At a variable t_0, which is the case for tracks by particles not correlated to the bunches (HClk) of the beams, the goal for the trigger timing is its activity at t_0. This suggests the investigation of the relative

[5] ceil(x): the smallest integer number greater than or equal x,
$\Theta(x)$: the Heaviside function

timing of the trigger w.r.t. t_0. In contrast to $bc_{\text{trig}}(t_{\text{det}})$, this is not any longer an integer function:

$$t_{0,\text{rel}} = bc_{\text{trig}}(t_{\text{det}}) - t_0 \tag{5.6}$$

According to the definition of t_{det} (equation 5.1), $t_{0,\text{rel}}$ is approximately equal to zero for small times $(t_{\text{det}} - t_0)$ from the muon's generation to its earliest detection in one of the module's trigger layers. [6]
Before the influence of the parameters t_{synch} and t_{resynch} on the trigger timing are simulated, the dependence of $t_{0,\text{rel}}$ on $\sigma_0(t_{\text{det}})$ has to be understood.
Figures 5.7a)–c) show the simulated distribution of $t_{0,\text{rel}}$ for three different widths of a uniformly distributed t_{det} (10ns, 70ns, 130ns). The t_0 was also assumed to be uniformly distributed between $t_0 = -0.5$bc and $t_0 = 0.5$bc and the phases t_{synch} and t_{resynch} were set to constant values ($t_{\text{synch}} = 90$ns and $t_{\text{resynch}} = 95$ns). The mean value of $t_{0,\text{rel}}$ is shifted to larger values for larger $\sigma_0(t_{\text{det}})$ since the width of the entire distribution is increased by larger detection times in this direction exclusively. As already discussed, for $\sigma_0(t_{\text{det}}) > 1$bc, it is impossible to measure the trigger signal always in the t_0–bc. Consequently, the increasing width of the distribution of $t_{0,\text{rel}}$ ($p(t_{0,\text{rel}})$) in figures 5.7a)–c) means a decreasing probability to do so.

The TE signals have a length of one bc. So the determination of the probability to observe the trigger in the t_0–bc can be achieved by the measurement of $t_{0,\text{rel}} = bc_{\text{trig}} - t_0$ with the information on bc_{trig} determined by the position of the respective trigger data bit in $2n+1$ GPTP pipelines, for which t_{GPTP} differs by 1 bc from pipeline to pipeline. The quotient (efficiency) distribution [7]

$$\varepsilon(t_{0,\text{rel}}) = \frac{(2n+1)\; p_{t_{0,\text{rel}}}(t_{0,\text{rel}})}{\sum_{t_{\text{GPTP}}=-n}^{t_{\text{GPTP}}=+n} p_{t_{0,\text{rel}}}(t_{0,\text{rel}} + t_{\text{GPTP}}) + \varepsilon} \tag{5.7}$$

contains the information on the probability of the TE activity at t_0.

Due to the length of the TEs of 1 bc, this is a box distribution of width 1 bc around the mean value $\bar{t}_{0,\text{rel}} = (t_{0,\text{rel.,max}} - t_{0,\text{rel.,min}})/2$, which is smeared by $\sigma(t_{\text{det}})$.
For a gaussian distributed $t_{0,\text{rel}}$ it is described by [8]

$$\varepsilon(t_{0,\text{rel}}) = \frac{1}{4}\, \mathrm{G}((-0.5 + (t_{0,\text{rel}} - \bar{t}_{0,\text{rel}}))/\sigma(t_{\text{det}}))\; \mathrm{G}((-0.5 - (t_{0,\text{rel}} - \bar{t}_{0,\text{rel}}))/\sigma(t_{\text{det}})). \tag{5.8}$$

Figures 5.8 a)–c) show the efficiency distributions corresponding to figures 5.7 a)–c). For $\sigma_0(t_{\text{det}}) = 10$ns one approximately receives the theoretical optimum of the box distribution. For $\sigma_0(t_{\text{det}}) = 70$ns the peak efficiency is still equal to one, but the plateau width, which shall be defined by 95% of the peak efficiency, has decreased to about 0.3 bc. For $\sigma(t_{\text{det}}) > 96\text{ns} = 1$bc the peak efficiency is lower than 1 but with further on increasing values of $\sigma_0(t_{\text{det}})$, the plateau becomes wider again. This effect is due to the assumed uniform distributions of t_0 and t_{det}.
As already shown in figure 5.1, the distribution of bc_{trig} is highly influenceable by the phases t_{synch} and t_{resynch} of the (re)synchronising HClk derivates w.r.t. $t_0 = 0$ on the

[6] Here, t_{synch} is assumed to define the observation of the trigger in bc 0. If not, this can easily be achieved by a respective change of t_{MPSDC} or t_{GPTP}.
[7] $0 < \varepsilon \ll 1$ to avoid formally divisions by zero.
[8] Here $G(x)$ is the Gaussian error integral defined by $G(x) = \frac{1}{2\pi}\int_{-\infty}^{x} dt\; exp(-x^2/2)$

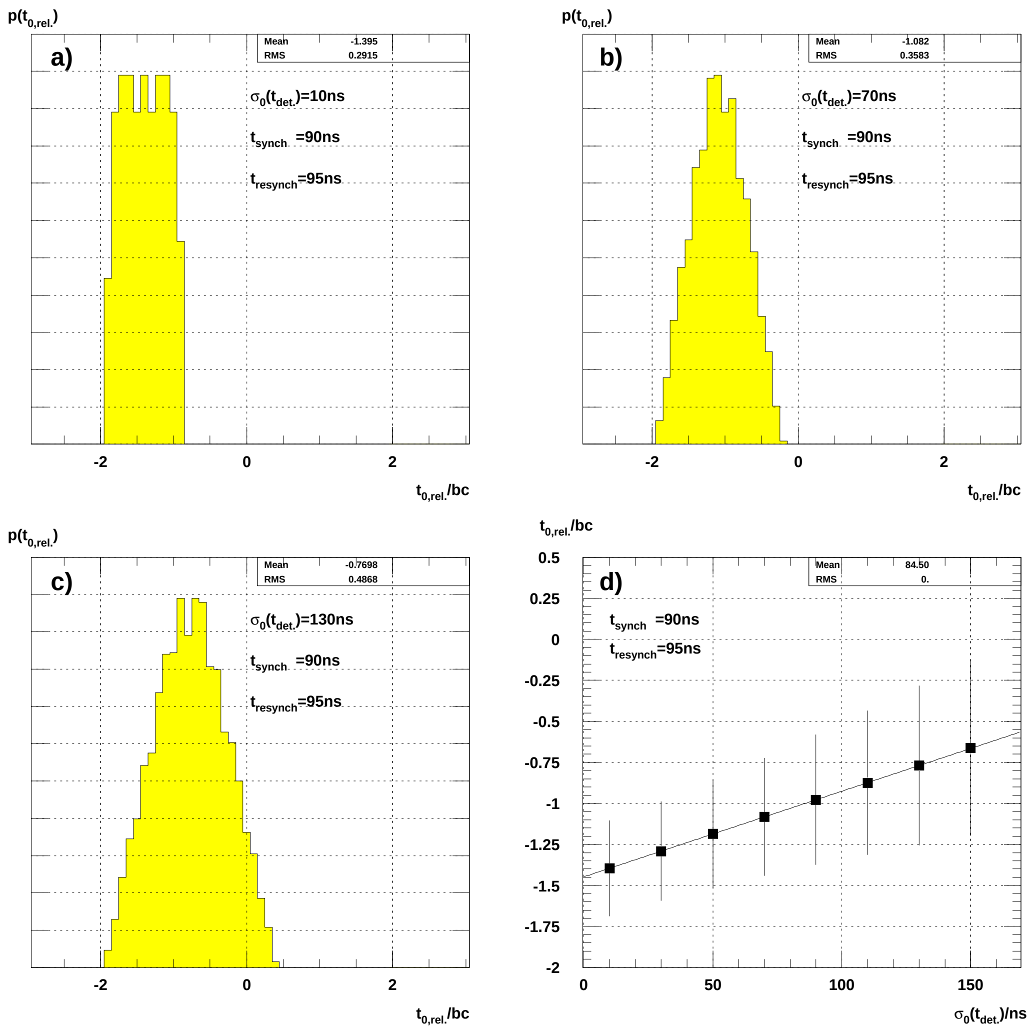

Figure 5.7.: a)–c): Simulated distributions of $t_{0,\mathrm{rel}}$ for three different values of $\sigma_0(t_{\mathrm{det}})$ and constant t_{synch} and t_{resynch}. Figure d) shows the mean $t_{0,\mathrm{rel}}$ vs $\sigma_0(t_{\mathrm{det}})$ for $10\mathrm{ns} \leq \sigma_0(t_{\mathrm{det}}) \leq 150\mathrm{ns}$.

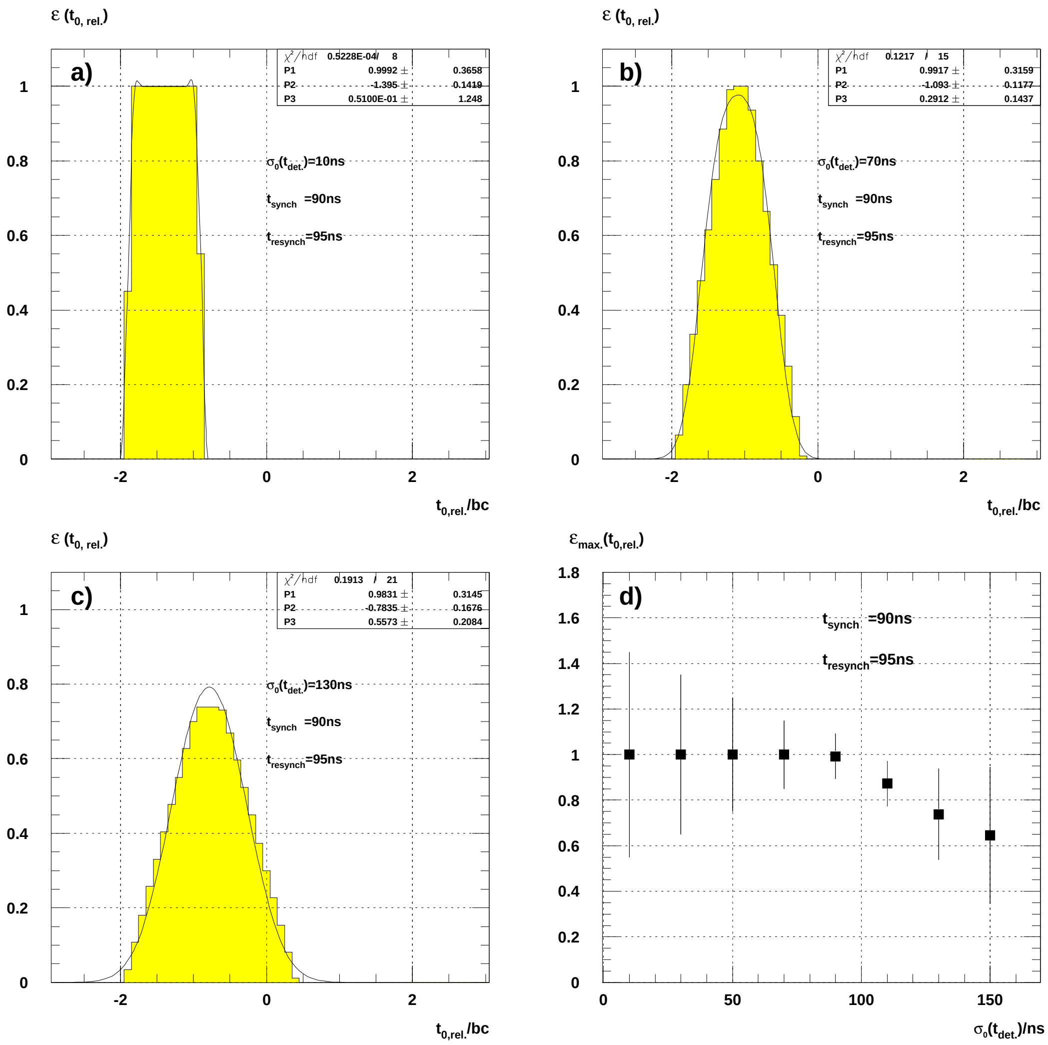

Figure 5.8.: a)–c): Simulated dependence of the t_0 efficiency $\varepsilon(t_{0,\mathrm{rel}})$ on $\sigma_0(t_{\mathrm{det}})$ for three different values of $\sigma_0(t_{\mathrm{det}})$ and constant t_{synch} and t_{resynch}. Figure d) shows the maximum $\varepsilon(t_{0,\mathrm{rel}})$ vs $\sigma_0(t_{\mathrm{det}})$ for 10ns $\leq \sigma_0(t_{\mathrm{det}}) \leq$ 150ns. The error bar here indicates the width of the plateau (defined as $\geq$ .95% of the maximum $\varepsilon(t_{0,\mathrm{rel}})$)

WDMB respectively on the MPSDC. Consequently their influence on the distribution of $t_{0,\mathrm{rel}}$ is the same.
Figures 5.9 to 5.12 show the dependence of the mean value of $t_{0,\mathrm{rel}}$ on t_{synch} simulated for four different widths $\sigma(t_{\mathrm{det}})$ and four different phases t_{resynch}.
Independent of $\sigma_0(t_{\mathrm{det}})$, for larger t_{synch}, the mean $t_{0,\mathrm{rel}}$ is shifted into the past. This behaviour can be expected from figure 5.1, since due to the later synchronisation, more triggers from streamers with larger drift times are assigned to the earlier bc. The peak efficiency is not affected by this as derivable from the distributions of $\varepsilon(t_{0,\mathrm{rel}})$ for $\sigma_0(t_{\mathrm{det}}) = 90\mathrm{ns}$ and $t_{\mathrm{resynch}} = 45\mathrm{ns}$ in figure 5.13.
The discontinuity at $t_{\mathrm{synch}} = t_{\mathrm{resynch}}$ corresponds to the term $\Theta[(t_{\mathrm{synch}}$ modulo $1) - (t_{\mathrm{resynch}}$ modulo $1)]$ in equation 5.6. So the dependence of the mean $t_{0,\mathrm{rel}}$ on t_{synch} for the assumed uniform distributions of t_0 and t_{det} can be described by the following saw function:

$$\bar{t}_{0,\mathrm{rel}}(t_{\mathrm{synch}}, t_{\mathrm{resynch}}) = \Theta\left[(t_{\mathrm{synch}} \text{ modulo } 1) - (t_{\mathrm{resynch}} \text{ modulo } 1)\right] - t_{\mathrm{synch}} \text{ modulo } 1 \quad (5.9)$$

If t_{det} is distributed asymmetrically, with a tail to larger t_{det}, this tail is also observed in the distribution of $t_{0,\mathrm{rel}}$. From figures 5.9 to 5.12 it can be concluded for the possibility of the calibration of the trigger timing that theoretically, there exist *several* sets $(t_{\mathrm{synch}}, t_{\mathrm{resynch}})$ for which the mean value of $t_{0,\mathrm{rel}}$ is equal to an integer number of bc k, which allows to correct the timing (if $k \neq 0$) by means of the delay t_{MPSDC}. In reality, many of these combinations solving the Central–μ–Trigger timing problem are forbidden either for reasons of electronic security (phases of signals to (re)synchronising HClks) or incompatibility with the aims of the timing of the read out.

5.3. The Calibration

5.3.1. Preadjustments

A few general adjustments on the trigger electronics have to be made before a fine tuning of the timing is reasonable. To minimise electronic inefficiencies, the following signals have to be stable 20ns before validation (in the same order):

1. the phase of the LB input (WDMB output) signals to the resynchronising LB HClk, to be adjusted for all 12/13 LBs with the HClk delay on the Clock Receiver Card in the LB crate

2. the phase of the MPSDC input (LB output) signals to the resynchronising MPSDC HClk, to be adjusted with the LB output delay on each LB and the HClk delay on the H1MPSDC

3. the phase of the SB input (H1MPSDC output) signals to the resynchronising SB HClk , to be adjusted for all H1MPSDCs with the HClk delay on the Clock Receiver Card in the SB crate

4. the phase of the SB output HClk to the PEn put into the the GPTP, to be adjusted with the PEn delay on the Fan Out Board reserved for the SB crate

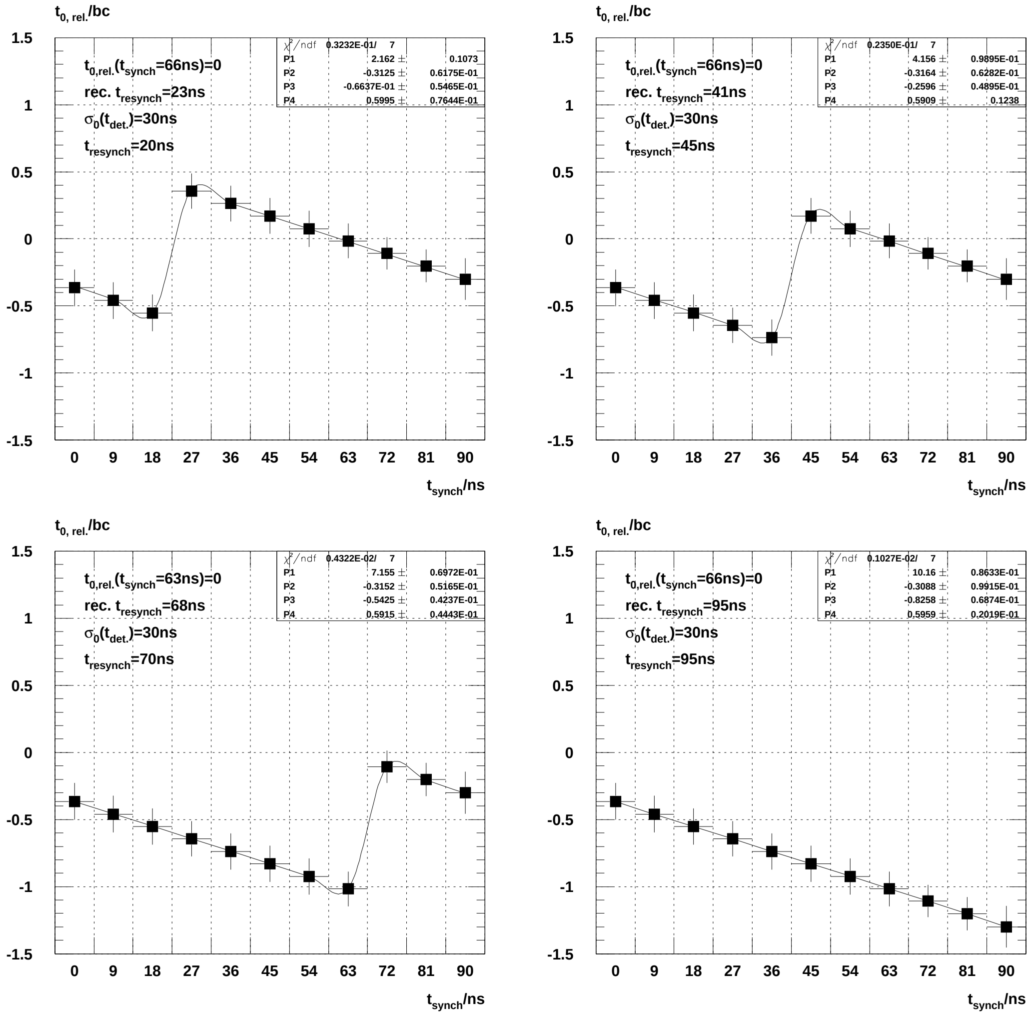

Figure 5.9.: Simulated dependence of the mean $t_{0,rel.}$ on t_{synch} for a uniformly distributed detection time t_{det} of width $\sigma_0(t_{\mathrm{det}}) = 30$ ns and four different phases of resynchronisation t_{resynch}. In addition, the reconstructed value of t_{resynch} is given. Errors give rms of mean $t_{0,\mathrm{rel}}$.

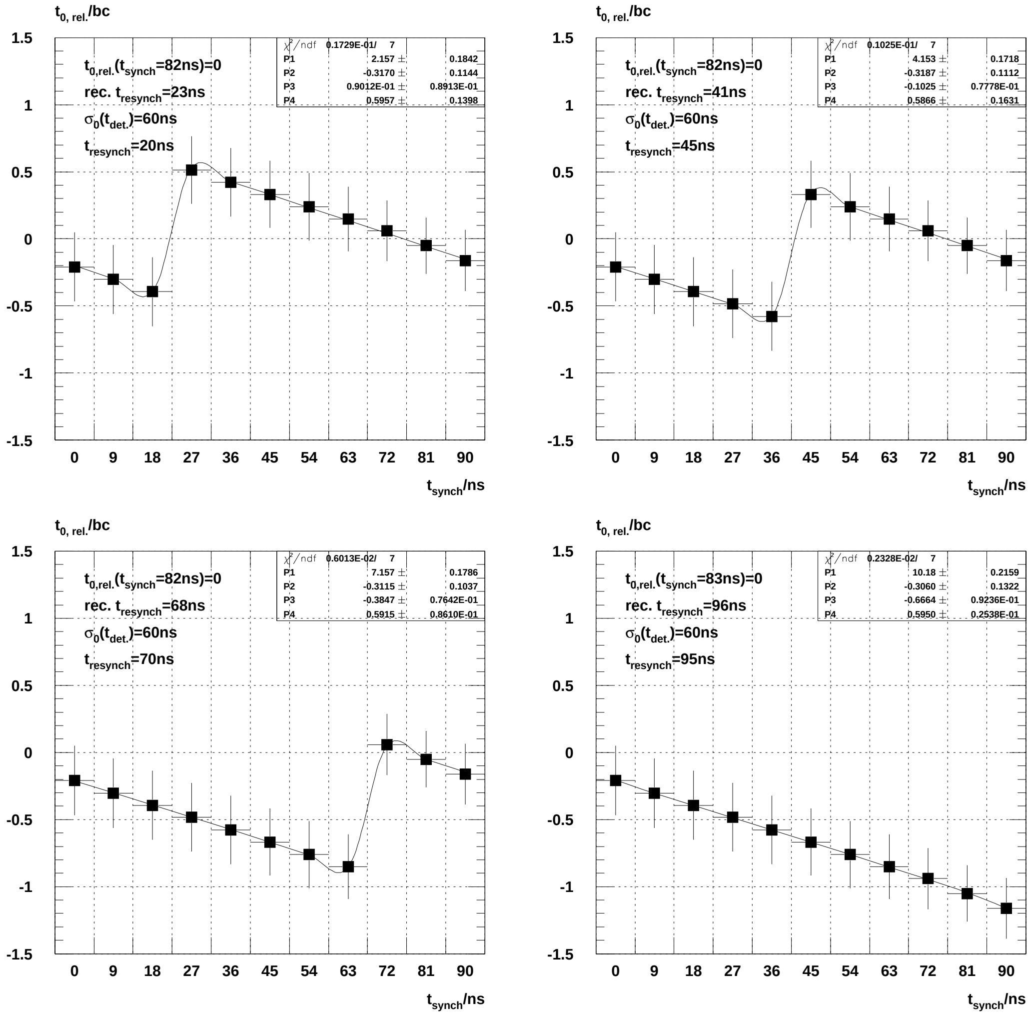

Figure 5.10.: Simulated dependence of the mean $t_{0,rel.}$ on t_{synch} for a uniformly distributed detection time t_{det} of width $\sigma_0(t_{\mathrm{det}}) = 60\mathrm{ns}$ and four different phases of resynchronisation t_{resynch}. In addition, the reconstructed value of t_{resynch} is given. Errors give rms of mean $t_{0,\mathrm{rel}}$.

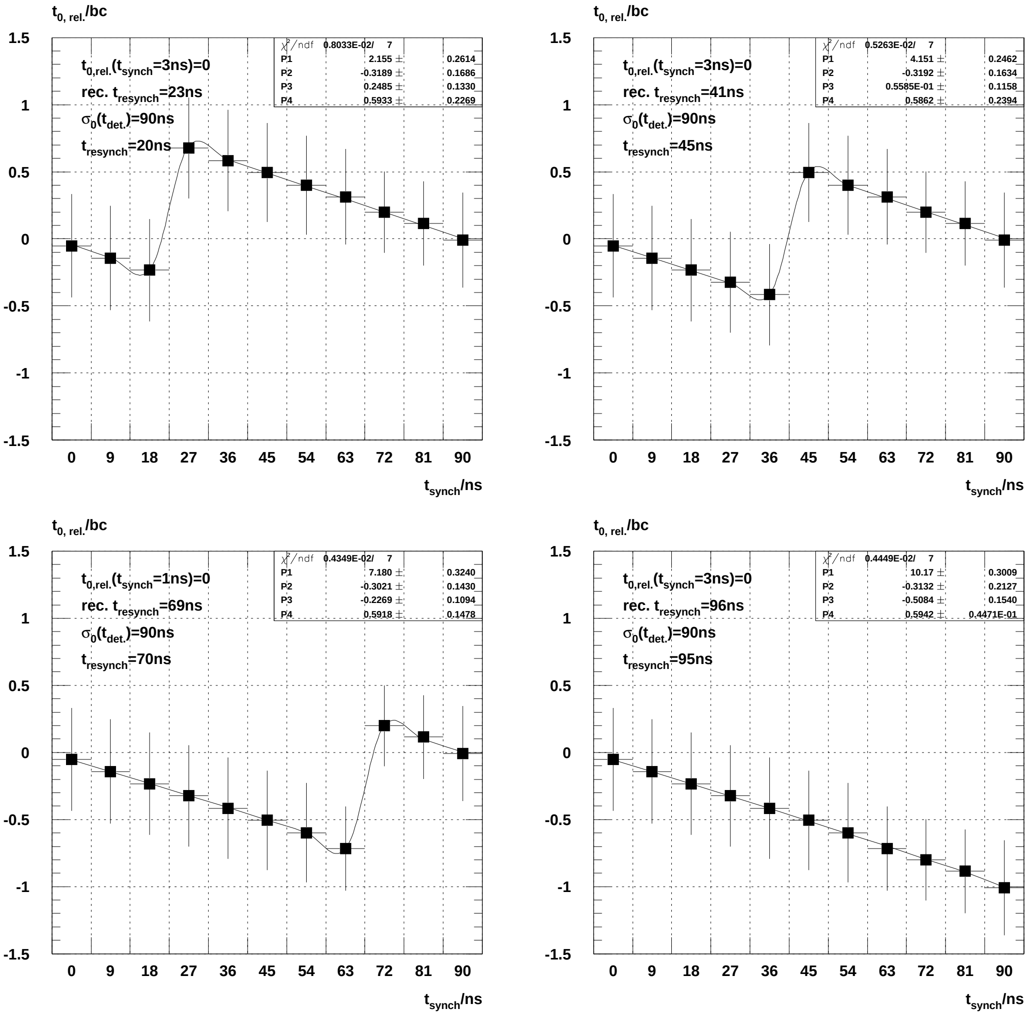

Figure 5.11.: Simulated dependence of the mean $t_{0,rel.}$ on t_{synch} for a uniformly distributed detection time t_{det} of width $\sigma_0(t_{\mathrm{det}}) = 90\mathrm{ns}$ and four different phases of resynchronisation t_{resynch}. In addition, the reconstructed value of t_{resynch} is given. Errors give rms of mean $t_{0,\mathrm{rel}}$.

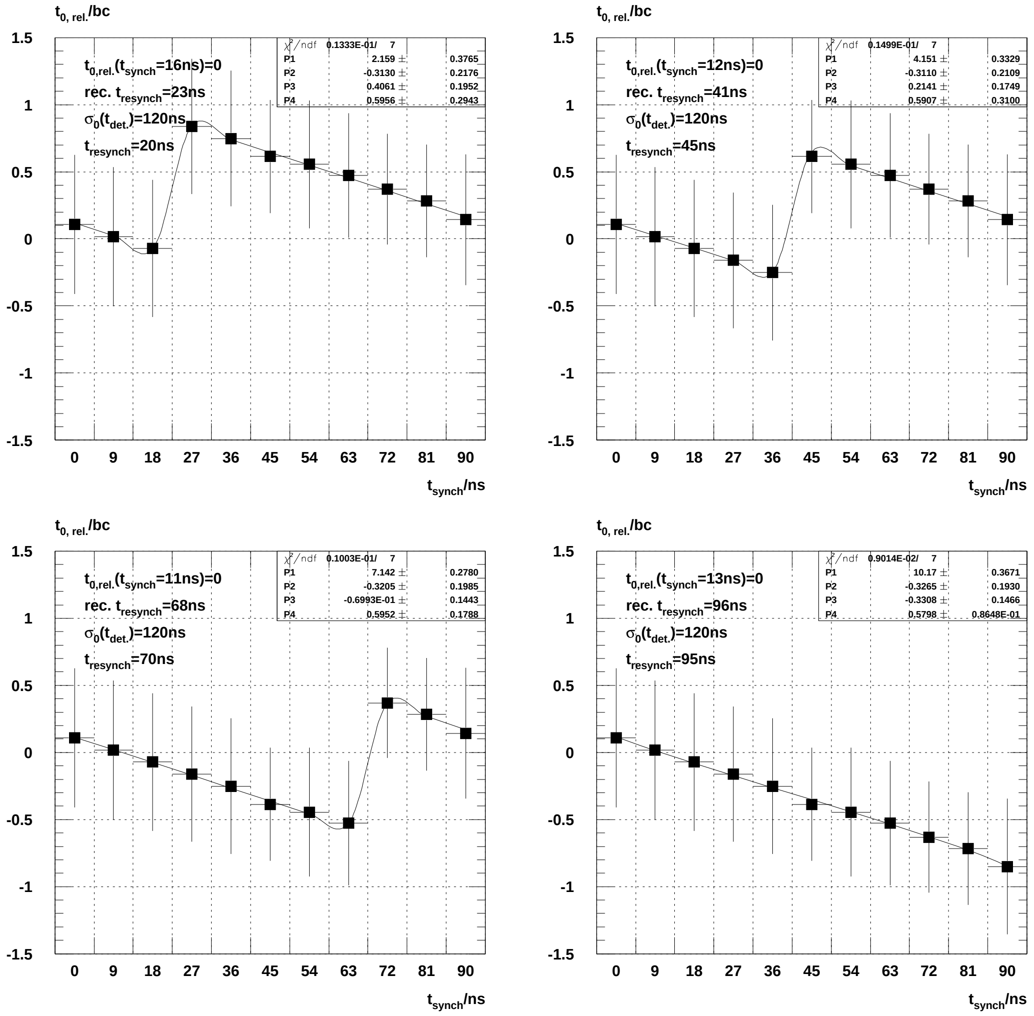

Figure 5.12.: Simulated dependence of the mean $t_{0,rel.}$ on t_{synch} for a uniformly distributed detection time t_{det} of width $\sigma_0(t_{\mathrm{det}}) = 120\mathrm{ns}$ and four different phases of resynchronisation t_{resynch}. In addition, the reconstructed value of t_{resynch} is given. Errors give rms of mean $t_{0,\mathrm{rel}}$.

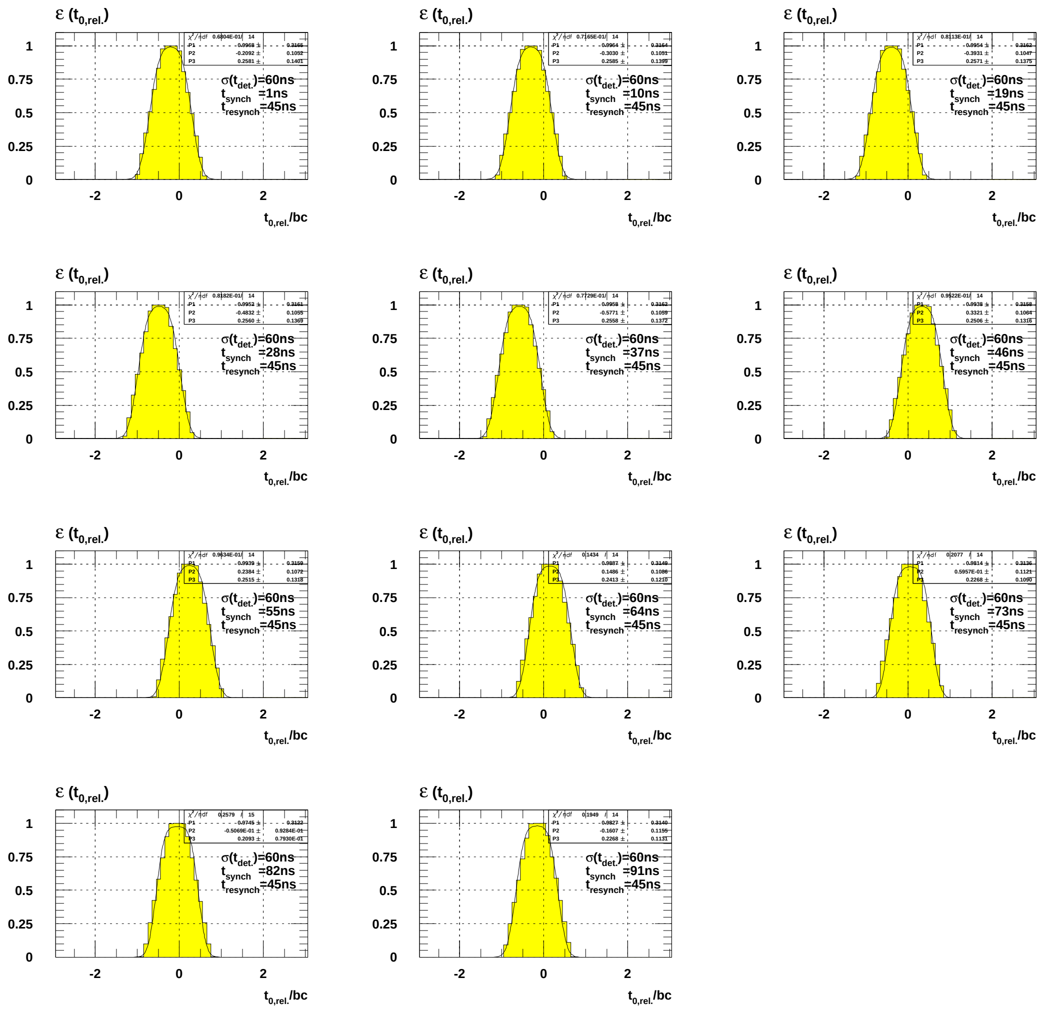

Figure 5.13.: Simulated $\varepsilon(t_{0,\mathrm{rel}})$ for a uniformly distributed t_{det} of width $\sigma_0(t_{\mathrm{det}}) = 60\mathrm{ns}$ for eleven different phases $1\mathrm{ns} \leq t_{\mathrm{synch}} \leq 91\mathrm{ns}$ and $t_{\mathrm{resynch}} = 45\mathrm{ns}$

After these basic adjustments, it is in principle possible to calibrate the timing of the trigger by shifting the edge of the synchronising HClk on the WDMBs by means of the delay on the Fan Out Cards.

5.3.2. The Calibration Data

In order to get not only a discrete distribution of the bc in which the triggers were observed by the CTL1, but a continuous information on the trigger timing, for the calibration bc_{trig} is measured for a variable t_0 as shown in the simulation. This means, one has to scan the time window around $t_0 = 0$ to be able to analyse the correlation between t_0 and t_{det} by correcting the measured bc_{trig} by t_0.
The main condition for this type of data is that during the data acquisition, the triggering muons must not be correlated to the active experiment HClk. This can be realised with muons from the cosmic radiation while using the HClk correlated to one of the beams as the experiment clock. Due to the trigger condition (CIP-4), the geometry of the Central–μ–Detector and the applied module trigger conditions, these muons for the most part illuminate the Barrel and the outer Endcap modules.
For the timing calibration of the modules in the Endcaps, the inner Endcaps in particular, it is comfortable to use muons from the proton beam halo, whose trajectories mostly have low angles ϑ. This promises a passage through the Endcap modules approximately perpendicular to the wire layers. In in this type of calibration data neither the HClk correlated to the proton beam nor that correlated to the positron beam is useful, since both have a constant phase to the triggering muons. Here a technical feature of the H1 trigger electronics becomes very useful: all trigger subsystems are able to generate their own artificial HClk. The frequency of this HClk differs by about 20 Hz from the nominal HClk provided to the experiments by HERA [38].
So using this artificial clock for the entire experiment guarantees that in all subdetectors the hits of the triggering muons have no constant phase to the proton clock and allows a scan of the entire t_0 time window. The reference times reconstructed from tracks in the CJC respectively the Forward Muon Detector, which indicate $t_0 = 0$ in luminosity runs are determined from luminosity data in case of the CJC, for the Forward Muon Detector from proton-HERA-clocked beam halo data (for reasons of higher rates and statistics). As figures 5.14 show, the widths of the measured distributions of the nominal t_0 reconstructed in both reference subdetectors are sufficiently small: ($\sigma_{\text{CJC}}(t_0) = 1.3\text{ns}$ and $\sigma_{\text{Fwd}\mu}(t_0) = 5.6\text{ns}$) to use the respective mean value as sharp reference value in the calibration. Figures 5.15 show t_0 distributions measured in calibration data. The t_0 reconstructed from cosmic muon tracks in the CJC is approximately uniformly distributed in a time window of width 1 bc. The fact that the mean t_0 is not equal 0 is again a consequence of different phases w.r.t. t_0 of the initially synchronising HClk for the CJC and the triggering CIP. The shape of the distribution of the t_0 reconstructed in the Forward–μ–Detector from muons in the proton beam halo is not yet completely understood [37], but has no influence on the results of the calibration measurements. The deviation of the t_0–distribution from a box of width 1 bc has a large influence on the shape of the $t_{0,\text{rel}}$–distributions but does not change neither the mean of the distribution of $\varepsilon(t_{0,\text{rel}})$ nor the accuracy, i.e. the width of the plateau. This has been simulated for a t_0 uniformly distributed with a width $\sigma(t_0) = 145\text{ns}$ (figure 5.16), and measured in a beam halo calibration run (figures 5.17).

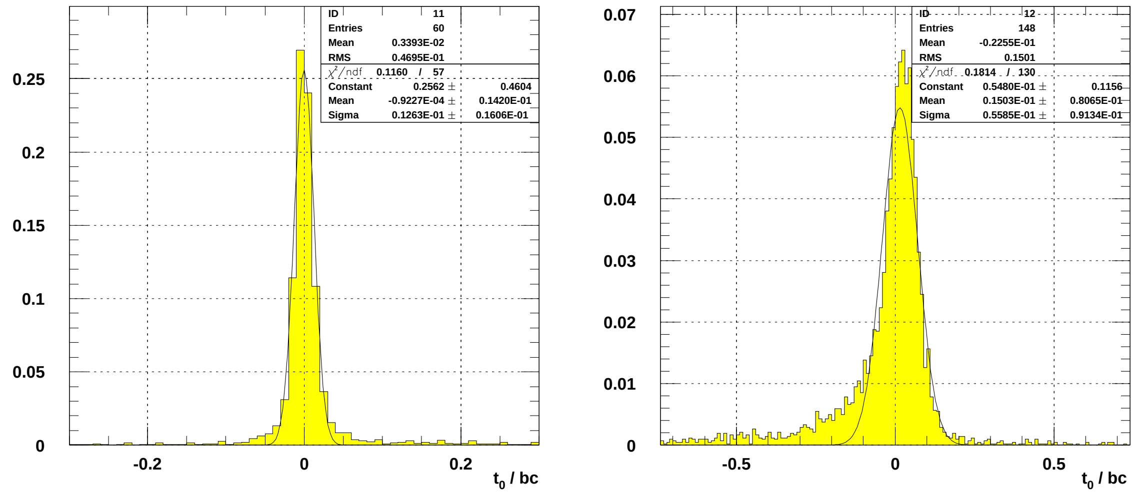

Figure 5.14.: Normalised distributions of the t_0 reconstructed in the CJC for luminosity data (left) and in the Forward–μ–Detector for beam halo data (right)

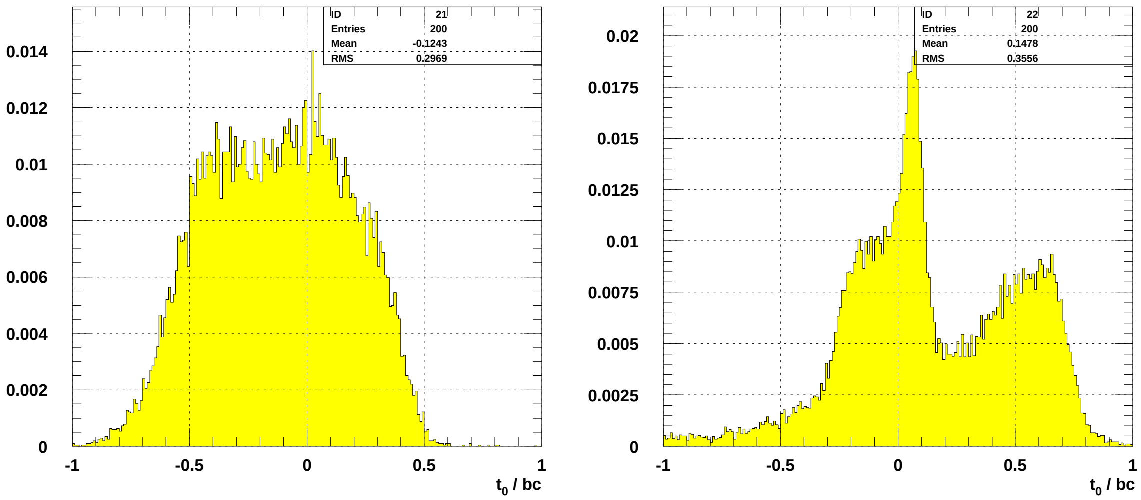

Figure 5.15.: Normalised distributions of the t_0 reconstructed in the CJC for CIP-4 cosmic data (left) and in the Forward μ Detector for beam halo data (right)

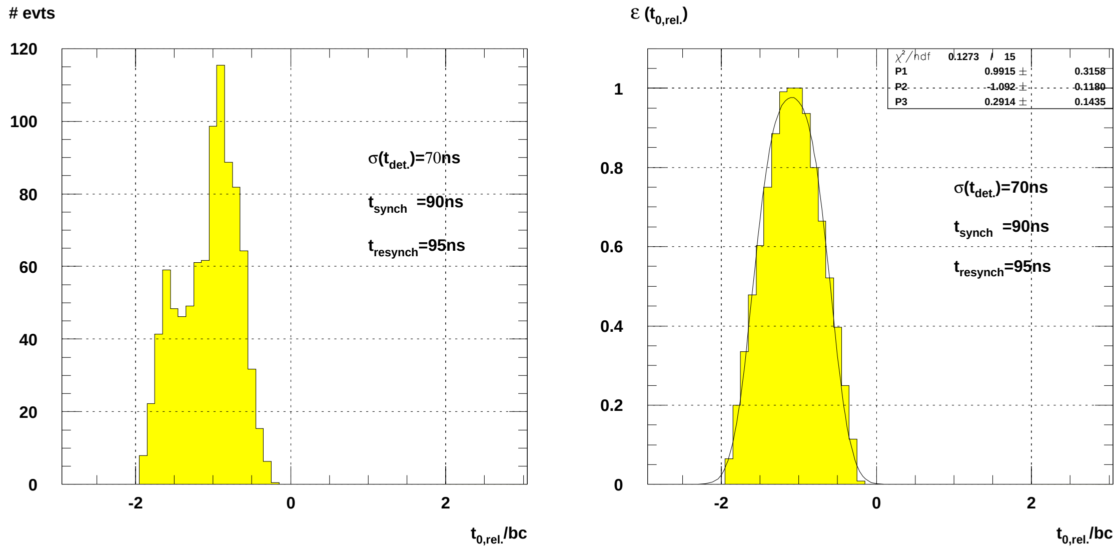

Figure 5.16.: Distributions of $t_{0,\mathrm{rel}}$ and $\varepsilon(t_{0,\mathrm{rel}})$ simulated for $\sigma(t_{\mathrm{det}}) = 70\mathrm{ns}$, $t_{\mathrm{synch}} = 90\mathrm{ns}$ and $t_{\mathrm{resynch}} = 95\mathrm{ns}$.

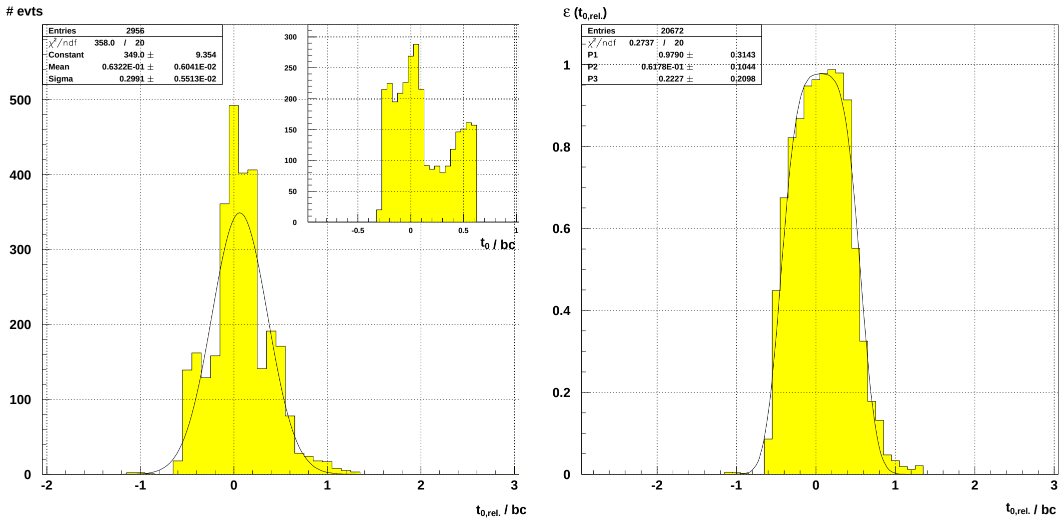

Figure 5.17.: Distributions of $t_{0,\mathrm{rel}}$ and the respective t_0 for TE Mu_FIEC activated by layer coincidences in module 55 (right) and the resulting distribution of $\varepsilon(t_{0,\mathrm{rel}})$ determined from beam halo calibration data.

5.3.3. Correction of Time of Flight t_{flight}

Assume a high energetic muon produced in an ep–collision at the vertex at the (reconstructed) time t_0 w.r.t. the time $t = 0$ defined by the L1AST which caused the event's read out. This muon passes the Central–μ–Detector at $t_{\text{flight}} = \frac{R}{c}$ later. Therefore, the first two terms in equation 5.1 can be combined to

$$t_{\text{pass,lumi}} = t_0 + t_{\text{flight}} = t_0 + \frac{R}{c}$$

For calibration data from the cosmic radiation or the proton beam halo, this is different, since on the one hand in these events, the muons which themself trigger the event, were *not* produced in the interaction region. On the other hand, the reconstruction of the interaction time t_0 is gauged on particles originating from the interaction region. This requires a correction t_{corr}:

$$t_{\text{pass,lumi}} = t_{\text{pass,calib}} + t_{\text{corr}} \tag{5.10}$$

Calibration data from the cosmic radiation are triggered with the CIP-4 ST. This means, in such events muons have to pass the CIP double layer twice to cause an L1K.

But the muons also pass the upper half ($y > 0$) of the Central–μ–Detector , *before* they pass the CJC, which provide the information on the t_0 and the CIP, which trigger the events (see figure 5.18). So one derives for $t_{\text{pass,cosmic}}$ the passage time in CIP4 triggered cosmic muon events, for the upper half of the Central–μ–Detector (upper Barrel and upper Endcaps):

$$t_{\text{pass,cosmic}} = t_0 - \frac{R_{\text{U}}}{c} \implies t_{\text{corr}} = \frac{2R_{\text{U}}}{c} \tag{5.11}$$

For the lower half of the Central–μ–Detector , the muons appear to originate from the vertex, as in muon events in standard luminosity runs:

$$t_{\text{pass,cosmic}} = t_0 + \frac{R_{\text{L}}}{c} \implies t_{\text{corr}} = 0 \tag{5.12}$$

In calibration data from the beam halo, which is triggered by a coincidence trigger of the Forward Muon Detector and the Veto walls (s63), the correction is done analogously The triggering muons pass the H1 detector from backward to forward. The event t_0 is reconstructed from tracks in the Forward Muon Detector. Here, the modules both in the FEC and in the BEC are passed by the triggering muon earlier than if the muon had originated from the interaction region:

For the Forward Endcap:

$$t_{\text{pass,beamhalo}} = t_0 + \frac{|z_{\text{FEC}}|}{c} = t_0 + \frac{z_{\text{FEC}}}{c} \implies t_{\text{corr}} = \frac{R - z_{\text{FEC}}}{c} \tag{5.13}$$

for the Backward Endcap:

$$t_{\text{pass,beamhalo}} = t_0 - \frac{|z_{\text{BEC}}|}{c} = t_0 + \frac{z_{\text{BEC}}}{c} \implies t_{\text{corr}} = \frac{R - z_{\text{BEC}}}{c} \tag{5.14}$$

and so conclusively for both Endcaps:

$$t_{\text{corr}} = \frac{R - z}{c} \tag{5.15}$$

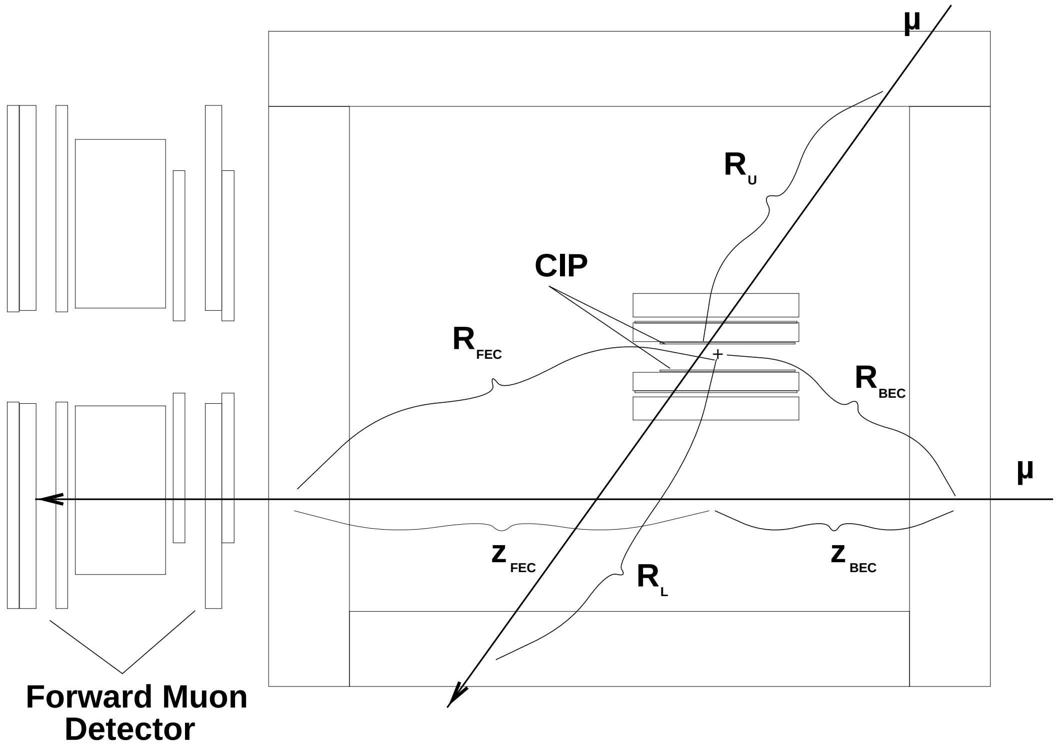

Figure 5.18.: Times of Flight to be considered in the calculation of the relative t_0 from cosmic and beam halo calibration muons

5.3.4. Calibration Measurements

The calibration aim is for all TEs originating from the 64 modules to fulfil the conditions

$$bc_{\text{trig,lumi}}(t_0 = 0) = 0 \;\; ; \;\; \varepsilon(t_{0,\text{rel}} = 0) = 1 \tag{5.16}$$

with t_0 measured in the reference subdetectors.
The module individual relative trigger timing, $t_{0,\text{rel}}$, is determined from the offline data, taking into account the correction on the time of flight t_{corr} via

$$t_{0,\text{rel}} = bc_{\text{trig,calib}} + t_{\text{corr}} - t_0 \; . \tag{5.17}$$

Since t_{synch} is the only parameter which allows a continuous tuning of $t_{0,\text{rel}}$ and $\varepsilon(t_{0,\text{rel}})$, calibration data are acquired for several different phases t_{synch}.
This is realised by changing the delay of the HClk provided to the cluster crates by the Fan Out Cards (compare section 5.1.3) within the entire possible time window of 1 bc.
In order to investigate the trigger timing behaviour of all modules separately it is necessary to resolve the ambiguity of the TEs (Mu_XIEC: sixfold, Mu_XOEC: tenfold, Mu_Bar: 32-fold (!)). Since the topology of 1–μ–events in cosmic and beam halo calibration runs is quite well known (see also chapter 7), it is sufficient to resolve it from TE to trigger sector level.
The information on the coincidence and the t_0–signals on trigger sector level is contained in the GPTP monitor pipelines which is read out and stored for each event. The remaining sixfold and eightfold module ambiguity of the sector trigger signals is resolved by means of the trigger simulation (see chapter 8).
For the determination of the module individual $t_{0,\text{rel}}$, only events are considered for which in maximal two different trigger sectors exactly one module–t_0–signal can be simulated. Furthermore a cut on the error of the reconstructed t_0 can guarantee its correct reconstruction.
The correction t_{corr} of the time of flight is calculated from the mean coordinates of the hit wires in the innermost hit trigger layer and the nearest hit strip. If no digital strip signal was observed, the mean value of t_{corr} for the module is applied.

Figure 5.19 shows the dependence of the mean $t_{0,\text{rel}}$ on t_{synch} measured in a set of cosmic calibration runs, each acquired with a different value of t_{synch}. The absolute value of t_{synch} is unknown, but of no relevance, since the aim of the variation of t_{synch} is the determination of a dublett (t_{synch}, t_{resynch}) for which the efficiency $\varepsilon(t_{0,\text{rel}})$ of $t_{0,\text{rel}}$ is maximal at $t_{0,\text{rel}}$ equal to an integer number of bc.
For the module in the example $t_{\text{synch}} = 18$ns fulfils this aim very satisfactory without any additional necessity to change t_{resynch}. Figures 5.20 show the measured distributions of $t_{0,\text{rel}}$ and the corresponding efficiency $\varepsilon(t_{0,\text{rel}})$ for this value of t_{synch}.
Due to the almost uniformly distributed t_0 in cosmic calibration data (compare figure 5.14), the distribution of $t_{0,\text{rel}}$ is approximately symmetric apart from a negligible tail to larger $t_{0,\text{rel}}$, originating from the tail of the drift time distribution. The width $\sigma_0(t_{\text{det}})$ fitted from the measured distribution of $\varepsilon(t_{0,\text{rel}})$ (compare equation 5.8) and the maximum value of $\varepsilon(t_{0,\text{rel}})$ nicely agree with the low probability that a module–t_0–signal is activated by streamer from the tail of the drift time distribution.
Figures 5.21 and 5.22 show the mean $t_{0,\text{rel}}$ and the respective $\varepsilon(t_{0,\text{rel}} = 0)$ calculated for

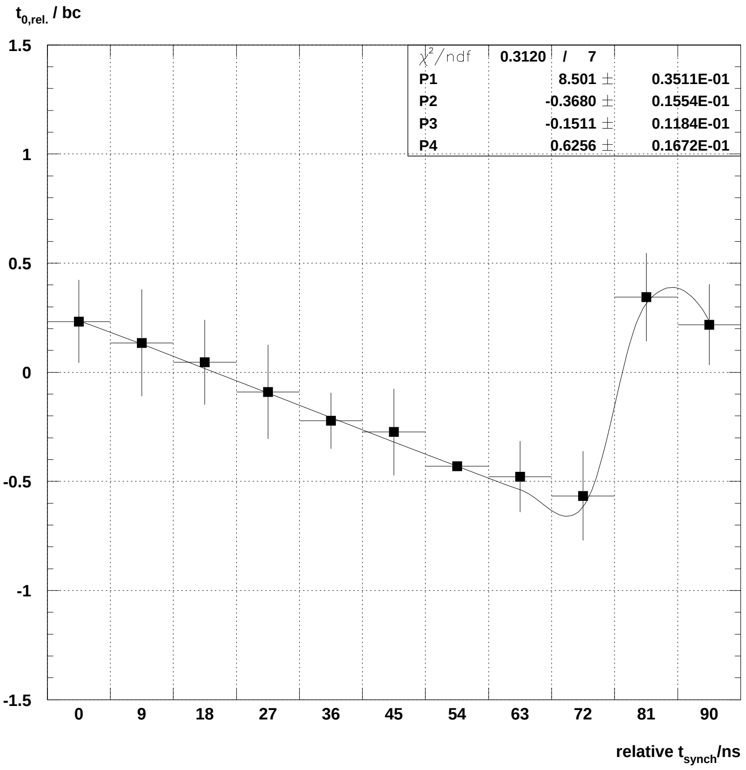

Figure 5.19.: Dependence of the mean $t_{0,\mathrm{rel}}$ on t_{synch} for triggers from module 28 in calibration runs. t_{synch} here has to be understood as $t_{\mathrm{synch}} + const.$, with an unknown constant

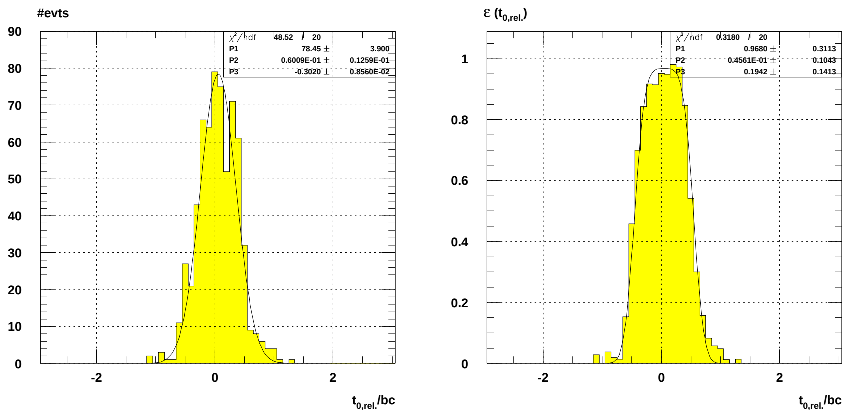

Figure 5.20.: $t_{0,\mathrm{rel}}$ and $\varepsilon(t_{0,\mathrm{rel}})$ for TE Mu_Bar activated by a layer coincidence in module 28 (cosmic calibration data)

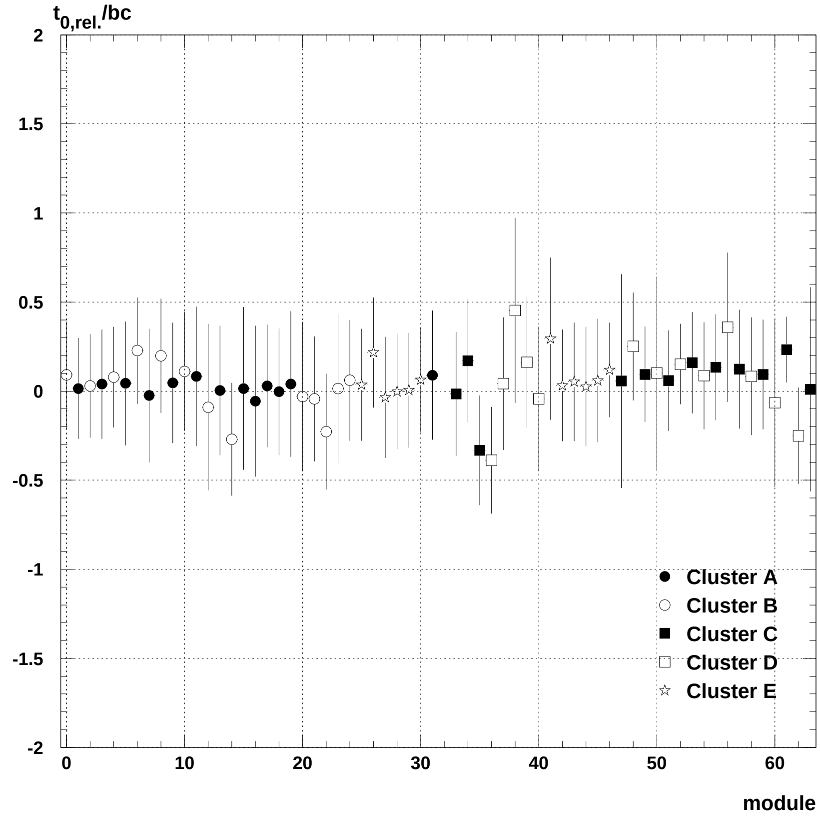

Figure 5.21.: The mean $t_{0,\mathrm{rel}}$ for each single module derived from cosmic and beam halo calibration runs.

each module separately. The values determined for t_{synch} for the five clusters lead to a satisfactory efficiency $\varepsilon(t_{0,\mathrm{rel}} = 0)$.

For part of the modules assigned to hardware cluster D the mean $t_{0,\mathrm{rel}}$ and therefore the plateau position of $\varepsilon(t_{0,\mathrm{rel}})$ are shifted to larger values. The reasons are on the one hand the bad compatibility of the trigger timing in the Barrel part and the FEC part of cluster D due to very different cable lengths. Due to this length, t_{synch} has to be chosen in a way, that all relevant data are still available in the read out pipeline at L1K. This is not the case for the t_{synch} for this cluster preferred by the trigger branch of the Central–μ–Detector . As intended, for most of these modules, $\varepsilon(t_{0,\mathrm{rel}})$ is maximised to at least 85% by means of decreasing t_{MPSDC} by 1bc.

The system constraint of the clusterwise change of t_{synch} in particular becomes visible for modules 35/36, for which nearly all characteristic values differ from those of the other modules of the same cluster (long wires, long cables s_{cluster} (fig. 5.6)). The mean $t_{0,\mathrm{rel}}$ and the plateau of $\varepsilon(t_{0,\mathrm{rel}})$ are positioned at about $t_0 = -0.4$bc. This cannot be corrected for by t_{MPSDC}: incrementing t_{MPSDC} by 1bc results in a mean value $t_{0,\mathrm{rel}} = +0.6$bc and a *lower* t_0–efficiency $\varepsilon(t_{0,\mathrm{rel}} = 0)$.

One can conclude that in principle the optimisation of the trigger timing is possible for each module individually, bot regarding the constraint given by the read out system. For

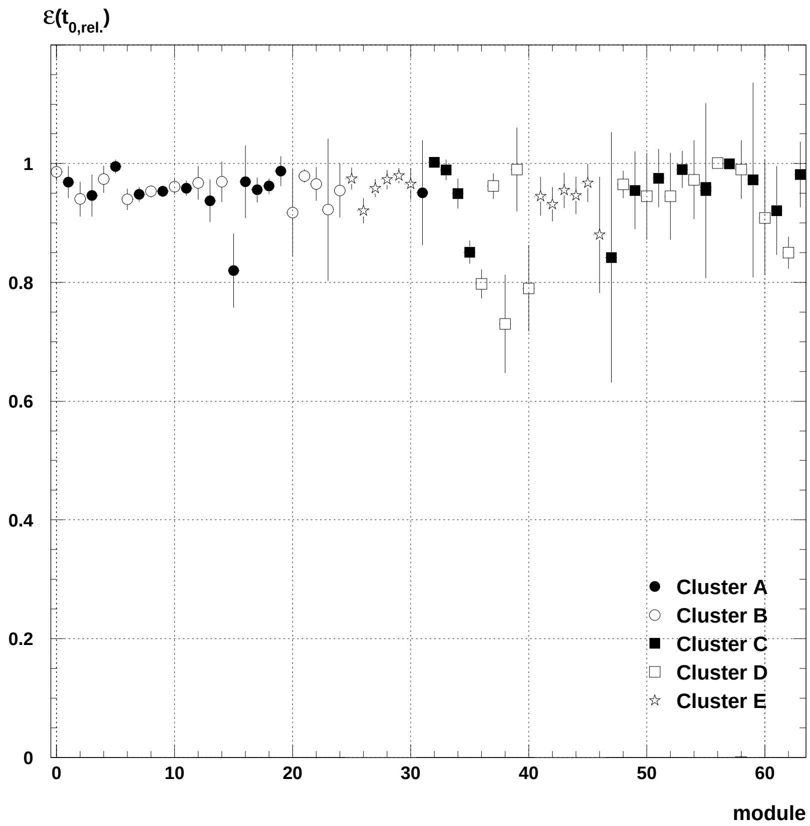

Figure 5.22.: The efficiency $\varepsilon(t_{0,\mathrm{rel}})$ at $t_{0,\mathrm{rel}} = 0$ for each single module derived from cosmic and beam halo calibration runs.

the chosen layer coincidences in each module, the influence of the width $\sigma_0(t_{\mathrm{det}})$ of the detection time on trigger t_0-efficiency $\varepsilon(t_{0,\mathrm{rel}})$ is negligible. In reality this possibility is limited since t_{synch} is changeable only clusterwise. In addition, the constraints of the read out branch of the Central–μ–Detector limit the applicable set of parameters.

For future detectors of this kind it is highly recommended to separate the readout and the trigger branch entirely. This means

- a separate synchronisation of the initial read out and trigger data
- individually adjustable signal phases for individual electronics
- an adjustment of the timing of both data and clock signals for all local detector segments
- an online monitoring of the phase of the initially synchronising HClk signals w.r.t. a reference HClk

6. Examples for multiple applicability and usage

6.1. Application of the Central–μ–Trigger electronics for a H1–BDC–Trigger

6.1.1. Compatibility

The BDC detector architecture is very similar to that of the Central–μ–Detector (compare section 1.7):

- drift cells instead of streamer tubes
- the number of channels is similar to that of one module of the Central–μ–Detector

In addition, the Central μ Trigger decision is based on programmable LUTs, so the hardware contains sufficient degrees of freedom for detector specific setups. This suggested the application of both the read out electronics of the Central–μ–Detector for the BDC's digital read out and the trigger electronics to derive a fast BDC trigger signal. So for the processing of the digital data no supplementary electronic hardware had to be developed.
The BDC consists of 2,048 drift cells, 256 per layer, 32 per octant. So one WDMB is able to process the data from the 16 wires of half an octant (see section 3.1) and 128 WDMBs are necessary to read out the entire detector.
To keep the granularity as small as possible (with this hardware), for the BDC the 8fold WORs of the WDMB were used as fast trigger output instead of the 16fold WOR (see section 3.3).
The ORing of the signals from 8 consecutive drift cells means a radial division of each layer into four rings of 8 cells width. These four rings further on will be called ϑ–Rings 0–3 (with increasing distance to the beam pipe).
It was decided to process the 256 fast WDMB trigger output signals in 8 Layer Boards (which have an input capacity of 400 signals). Since the BDC's aim is to improve the information on the ϑ of a particle track into the backward calorimeter, the eight WOR signals from the segments in the same ring in one layer are connected to one input port of an LB.

TE	meaning
0	3 of 4 layer–ANDs in ϑ–Ring 0
1	3 of 4 layer–ANDs in ϑ–Ring 1
2	3 of 4 layer–ANDs in ϑ–Ring 2
3	3 of 4 layer–ANDs in ϑ–Ring 3
4	3 of 4 layer–ORs in ϑ–Ring 0
5	3 of 4 layer–ORs in ϑ–Ring 1
6	3 of 4 layer–ORs in ϑ–Ring 2
7	3 of 4 layer–ORs in ϑ–Ring 3

Table 6.1.: The BDC Trigger Elements.

6.1.2. Setup of the Electronics

Following the same philosophy as for the Central–μ–Detector , i.e. triggering on multiple layer coincidences, the signals from the same ϑ–Ring of the adjacent second half of the double layer are connected to the same LB. By this assignment of input signals to LB, the latter became a Double Layer Board (DLB). Each DLB uses four input ports. Each input port receives the signals of one ϑ–ring. The WOR signals of two ϑ–rings of a double layer are connected to four input ports of one DLB. So in total there are eight DLBs installed in the system. The OR (SOR) of all sector signals connected to the same DLB input port represents the (digital) activity of any of the 64 cells in the respective ring.
For the BDC the same precaution has to be taken with respect to the maximal drift-time as for the Central–μ–Detector : the maximum drift time in a (big) BDC cell amounts to about 450ns and the digital signal length is fixed by the WDMBs to 96 ns (section 3.1), so the coincidental detection of two hits in both sides of a double layer is not guaranteed. Therefore the electronics for the elongation of the SOR signals had been modified in a way that signal lengths between 1 and 8 bc (in units of 1 bc) are programmable. This makes it possible to detect coincidences of SOR signals from the two halves of a double layer which originate from the same particle track. In order not to lose tracks, the logical OR of a segment is provided as well. The DLB LUT RAM output signals indicate if both ϑ–rings n were hit (AND–n) or at least one of the two (OR–n) of the double layer. The SB is used to detect coincidences of double layer signals concerning the same ϑ–ring, it is called a Main Coincidence Board (MCB). The conditions loaded to the MCB LUT RAMs require a multiplicity of 3 of 4 layer ANDs/ORs for each ϑ–ring. The GPTP Board is only used to delay and pipeline the trigger element byte before its transmission to the CTL1. So the eight MCB output bits at the same time are the final BDC Trigger Elements. Their meaning is given in table 6.1 The flow and the reduction of the BDC trigger data is illustrated in figure 6.1.

6.1.3. The Performance of the System

A system performance check is the trigger verification by comparison of real triggers and triggers simulated from the digital readout data with the help of a simulation package. Using the Central μ trigger electronics from the Central–μ–Detector consequently also the trigger simulation software package could be applied to the BDC. It consists of three

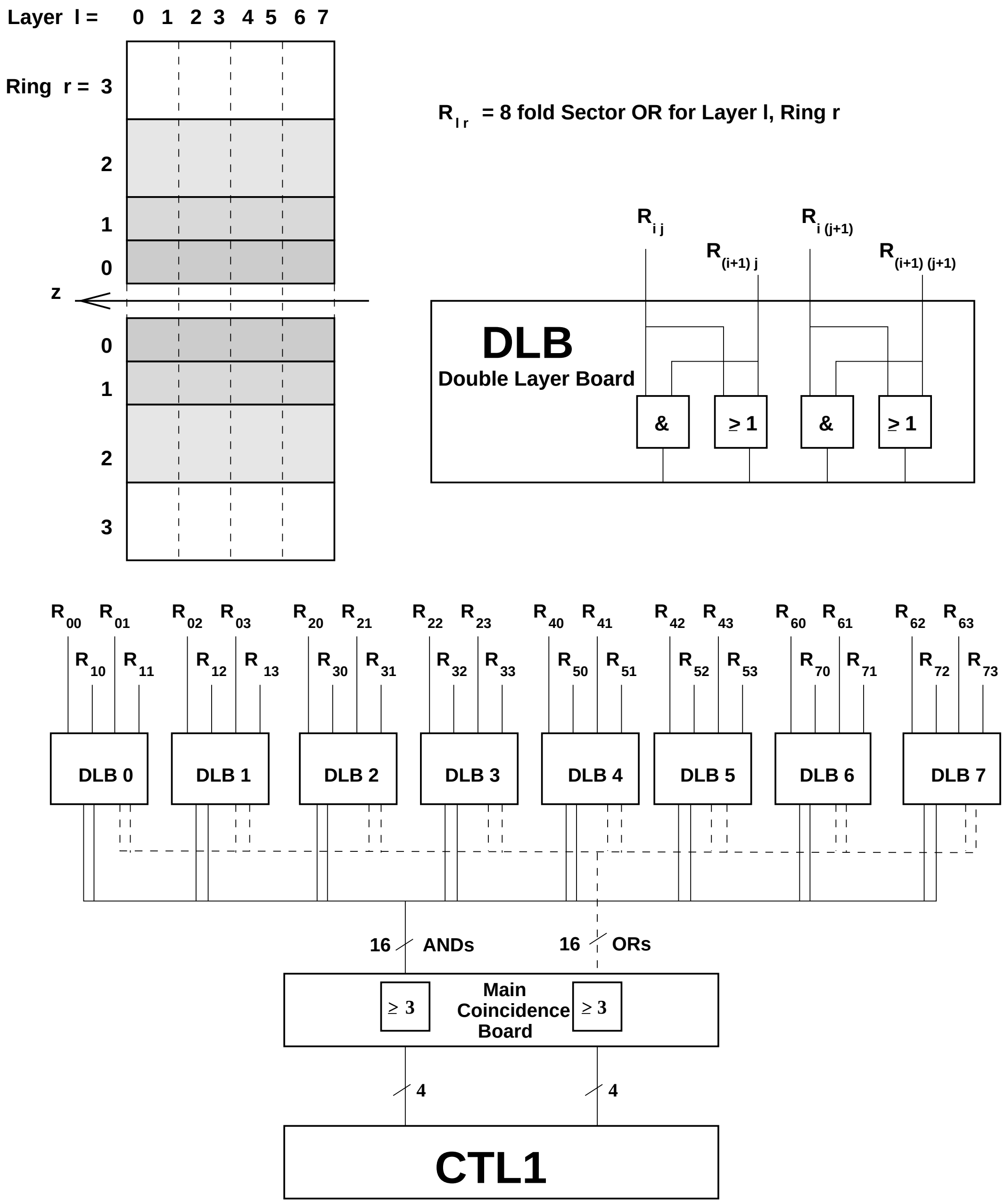

Figure 6.1.: Flow of the BDC trigger data from front end (WDMB) to CTL1

software modules which strictly simulate the electronics of the WDMBs, Double-Layer-Boards , and the Main Coincidence Board analog to the simulation of Central–μ–Trigger described in chapter 8.

The verification was done twofold:

A) Whenever TE n was active, it was tried to confirm this with the help of the digital readout data. The time structure could also be analysed because for both trigger and readout the data before and after the nominal t_0 bunch crossing is available.

B) Whenever the activity of TE n could be simulated from the digital readout data, it was tried to validate it from the real trigger data.

The results of test A are shown in figure 6.2. One observes a good correlation between simulation and data. The small deviations, especially in bc -5, are a consequence of the different time windows which were compared in the trigger and the readout data. In the trigger data one already observes elongated trigger signals, which have to be simulated from the readout data. If the initial signal is missing in the readout data, due to an insufficient time window, the trigger cannot be simulated for this bc.

The results of test B presented in figure 6.3 again show a good agreement in the shapes of the measured and simulated distributions. For TEs 0, 2 and 3 we do not observe a trigger signal in the data for each simulated trigger. This effect is of order 3–5%. The reason is not yet completely understood and still under investigation.

Due to the high synchrotron radiation background and the high efficiency of the BDC–trigger, the physics purity of the triggered events is regrettably very low, with higher beam quality and collimator efficiency this hopefully changes in the future. We can conclude that there are no BDC triggers (in bc 0) which cannot be simulated from the digital readout data, i.e. the trigger does not produce artificial signals. The timing of all eight BDC trigger elements seems to be adjusted very accurately: all distributions of the bc in which the respective TE is set show their maximum in bc 0.

6.2. Special Trigger Setups for the Calibration of other H1 Subdetectors

Due to its look–up table based logics, the Central–μ–Trigger is extraordinary flexible. Thus it can be used to trigger various different topologies not only during the acquisition of luminosity data but also for the necessary calibration of other H1 subdetectors. This means setups which exclusively trigger muons which most probably passed the subdetector the data is intended for. The reasons for these special setups can be different, chambers which are sensitive on synchrotron radiation during luminosity or which cannot even be switched on during injection/ramping of the beams, need an opportunity to acquire their calibration when their are no beams. Other detectors are calibrated with events of a certain topology which are triggered with a comparatively small rate. In the following, two examples are given for H1 subdetectors for which setups have been prepared which allow the fast acquisition of the individual cosmic calibration data.

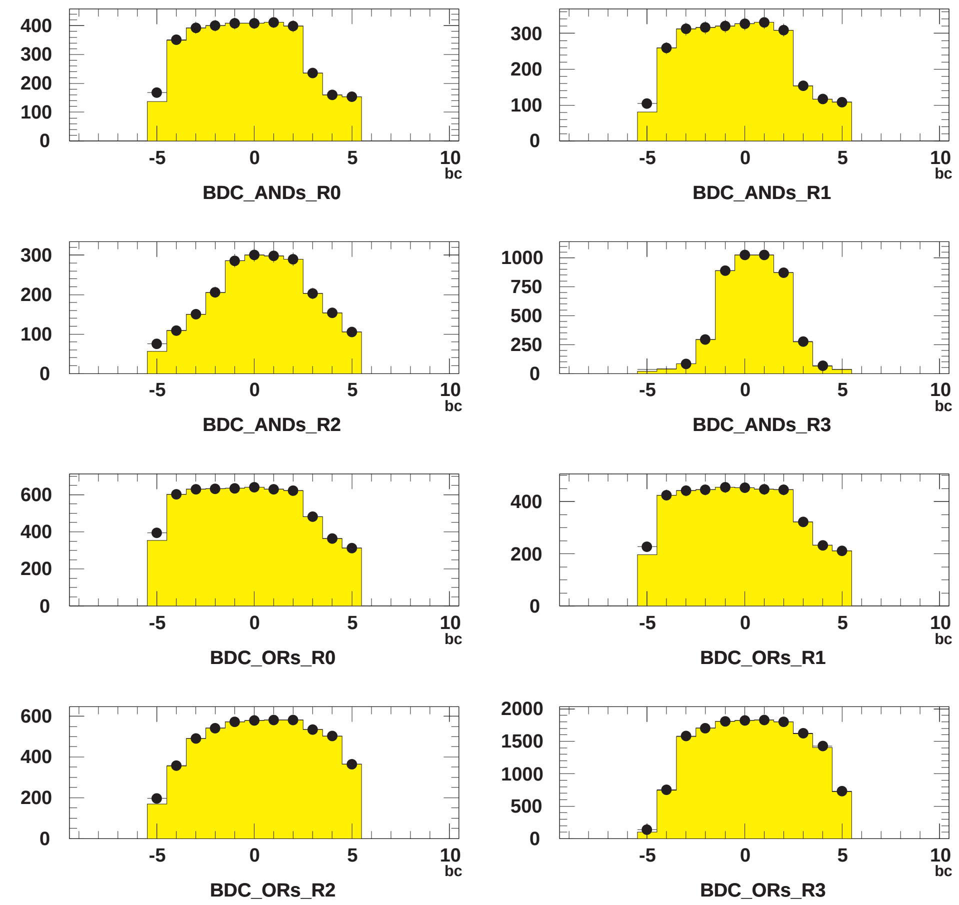

Figure 6.2.: Trigger verification type A, based on TE data (TEL1) of beam halo events triggered by the dedicated subtriggers (20 or 21): number of events with active TE vs. bunch-crossing (dots: real TE data, grey: triggers simulated from readout data).

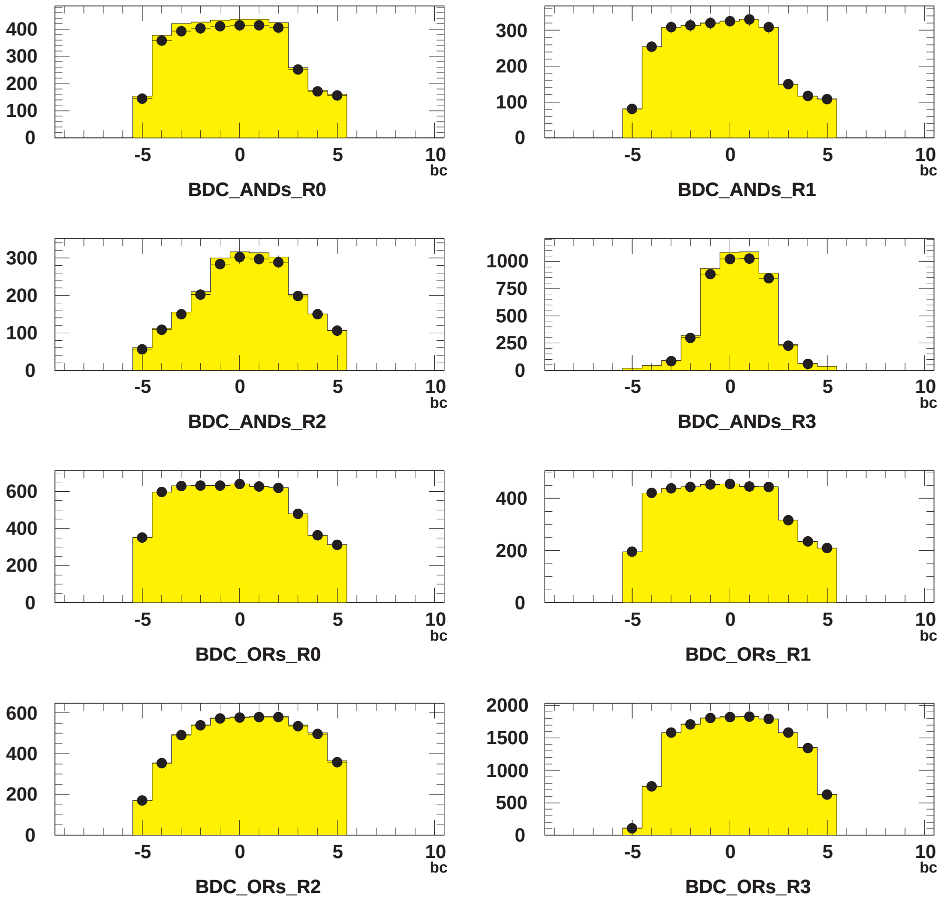

Figure 6.3.: Trigger verification type B, based on readout data of beam halo events triggered by dedicated subtriggers (20 or 21): number of events with active TE vs. bunch-crossing (dots: real TE data, grey: triggers simulated from readout data).

The rate R_μ of cosmic muons depends on the zenith angle $\vartheta_{\mathrm{zenith}}$, which in the H1 convention is the angle w.r.t. the y–axis. It is approximated by:

$$R_\mu(\vartheta_{\mathrm{zenith}}) \sim \cos^2 \vartheta_{\mathrm{zenith}} \tag{6.1}$$

The consequence is, that due to the first order dead time (section 2.1) the acquisition rate of calibration muon events with large $\vartheta_{\mathrm{zenith}}$ is very low. This is particularly uncomfortable in particular for H1 subdetectors dedicated to the extreme low and large ϑ region. Thus the special setups of the Central–μ–Trigger electronics serve as a limitation of the solid angle from which muon triggers are accepted.

6.2.1. A Cosmic Calibration for the BDC and the SpaCal

The BDC and the SpaCal approximately cover the polar angle region $153° < \vartheta < 177.5$. In order to trigger muons which probably pass the BDC/Spacal region, coincidences of sector triggers in the Backward Inner Endcap and the Forward Barrel or the Forward Endcap are suggested. The calibration setup for the Central Trigger offers two subtriggers (see appendix B)

s13=Mu_FEC_BEC=(Mu_BIEC||Mu_BOEC)&&(Mu_FIEC||Mu_FOEC) and
s14=Mu_BEC&&Mu_Bar=(Mu_BIEC||Mu_BOEC)&&Mu_Bar

which already express the desired conditions. So the SB LUT setup needs not to be changed: disabling the LB of the modules of the Backward Barrel and the Backward Outer Endcap leads the desired new meaning of s13 and s14. The disabling of the LBs can be done easily by means of the trigger control programme on the Macintosh supervising the Central–μ–Detector , in the H1 control room.

6.2.2. A Cosmic Calibration Trigger for the Tail Catcher Calorimeter

As for the calibration of the Central–μ–Trigger timing with CIP4 cosmic muons, for the Tail Catcher Calorimeter (TC) the rate of muons which pass the barrel modules with the wires parallel to the y–z plane (16, 23, 24, 31, 32, 39, 40, 47, compare figure 1.5) is very low. The rate of triggered events in these modules could be improved by disabling all other Barrel modules. But this is not yet sufficient, since the charge produced in the LST depends on the length of the muon track segment within the tube and therefore on φ and ϑ [9]. Along long track segments even more than one streamer is produced which complicates the detectors energy calibration. In order to gauge the TC energy measurement on muons passing the modules approximately perpendicular to the wire layers, one has to find trigger conditions which limit the possible range of both φ and ϑ. The azimuthal angular range covered by these problematic modules is $-22.5° < \varphi < 22.5°$ and $157.5° < \varphi < 205.5°$ This is approximately equivalent to $\vartheta_{\mathrm{zenith}} > 67.5°$ The interval of the azimuthal angle of the triggered muons can be limited by requiring a layer coincidence of layers three and twelve in the respective modules. The request of all five trigger layers would halve the trigger efficiency. All other modules of the Barrel are disabled again. In order to limit the polar angle of the desired muon tracks w.r.t the wire layers at least

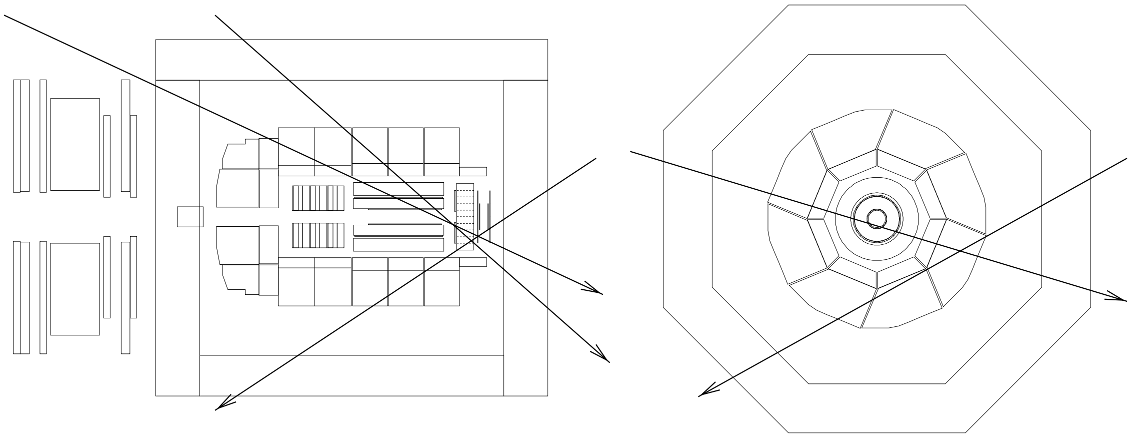

Figure 6.4.: Topologies triggered with the cosmic calibration setup for the BDC and the SpaCal (left) and for the Tail Catcher Calorimeter (right)

roughly [1], Barrel module coincidences are required which consider the signals of Forward and Backward Barrel separately. This allows only muons within a ϑ–window of $\pm 28°$. By means of this redefinition, the calibration subtrigger s4, Mu_2_Bar, of the serves to The change of the LUT contents in the LBs and SBs is realised by prepared LUTs which are easily selectable in the trigger control programme. With this setup, the subtrigger s4 Mu_2_Bar (in the calibration setup of the Central trigger) has the desired meaning.

Figure 6.4 depicts the triggered topologies for the two subdetectors.

[1]this is difficult due to wire lengths of 4.5m and the fact that the strips are not connected to the trigger

7. Rejection of Muon Background Events by means of the Central–μ–Trigger

The majority of non–collision–correlated background events in H1 originates from cosmic radiation, the proton beam halo and electron beam synchrotron radiation. In the following, investigations on the possibility to reject part of this background by means of the information provided by the Central–μ–Trigger system are presented.
Since the Central–μ–Trigger is unable to provide information on the origin of the triggered muon, it is necessary to get further information on the topology by a trigger in a supplementary trigger sector. On L1 one faces a 32fold module ambiguity of the TE Mu_Bar. The granularity of the other four sectors in the Endcaps is too large for statements on the origin of the triggered muon, too. So for further analysis it is suggested to use the module trigger information which is available on L2. On the one hand, this inhibits a reduction of the L1 input rate. On the other hand, the rejection of background events could either serve to decrease the L4 input rate and therefore lead to a reduction of the second order dead time or to decrease the L1 prescale factors in order to increase the rate of low rate physics triggers.
The intended rejection has to be restricted on events with two module triggers (layer coincidences), since on the one hand in events with only one module trigger, it is not guaranteed, that the second has been missed and the Central–μ–Trigger does not provide any information on a potential origin of the muon at all. On the other hand it is impossible to determine a correlation between triggers in more than two modules.

In events with two module triggers, it is at least possible to consider the angular correlation of the triggering modules, although without any precise information on the track direction. This can increase the confidence in the observation of a one–muon event from the background mentioned above.

7.1. Recognition of Cosmic and Proton Beam Halo Muons

As already shown in section 6.2, higher energetic cosmic muons passing through the vertex region most probably trigger modules back to back in φ. The trajectory of muons from the beam halo mostly is approximately parallel to beam line, so they are expected to trigger modules back to back in z. Offline these topologies can be filtered out by means of the hit information which allows a track fitting and so a comparison of the tracks in the

(two) modules. With the only available information on L2, the 64 layer coincidence bits from the modules, for the topology recognition of the events to be rejected, the regular numbering scheme of the modules (compare figure 1.5) proves as very useful. Figure 7.1 shows the distribution of the number of module triggers for explicit cosmic and proton beam halo data. The expected ratio of events with two module triggers for both data types is about 0.45.
In barrel cosmics events triggered by the CIP4 ST [1], the module triggers are expected to be back to back in φ. This means for the module number difference $\Delta\text{module} = |\text{module}_1 - \text{module}_2|$:

- $\Delta\text{module} = 8 \pm 1$, if both module triggers occurred in the same μ–subdetector or in the backward upper and forward lower barrel.
- $\Delta\text{module} = 24 \pm 1$, if the two module triggers occurred in forward upper and the backward lower barrel

The variation around the two values is a consequence of the track curvature due to the magnetic field. In beam halo muon events with one module trigger in each Endcap, the expectation is fulfilled that in both Endcaps modules with an equal local module number have triggered (see 1.1), which leads to a $\Delta\text{module} = 48$. The minor peaks at $\Delta\text{module} = 46$ and $\Delta\text{module} = 50$ result from muons with $\vartheta \neq 0$ (compare figure 1.5).

7.2. L4 Input Rate Reduction

To determine the order of magnitude of the L4 input rate reduction by means of a rejection of cosmic and beam halo muons, the fractions of events in which the L1ASTs were active and the above conditions for Δmodule were fulfilled have been determined.
The meaning of the respective L1ASTs can be looked up in appendix B. The fractions for barrel muons in general are below 15% except for s55. The fractions for beam halo muons for some subtriggers are above 60%. This is irrelevant for s20/s21 which are beam halo muon monitor triggers. Figures 7.3 and 7.4 show the rates of L1RSTs and L1ASTs which use an L1TE of the Central–μ–Detector in a luminosity run (in phase 2, i.e. still high beam currents and therefore higher L4 input rates). All rates are of order $\mathcal{O}$(Hz) are even lower. In addition the application of the investigated rejection could mean a sensitive cut into physics events, triggered by these low rate subtriggers.
Consequently, the rejection of background events based exclusively on the L2 information of the Central–μ–Detector fails. But the data it is used successfully in combination with the data from the other subdetectors both in L2NN and L2TT [40].

[1]This means also that the muons roughly pass the vertex region

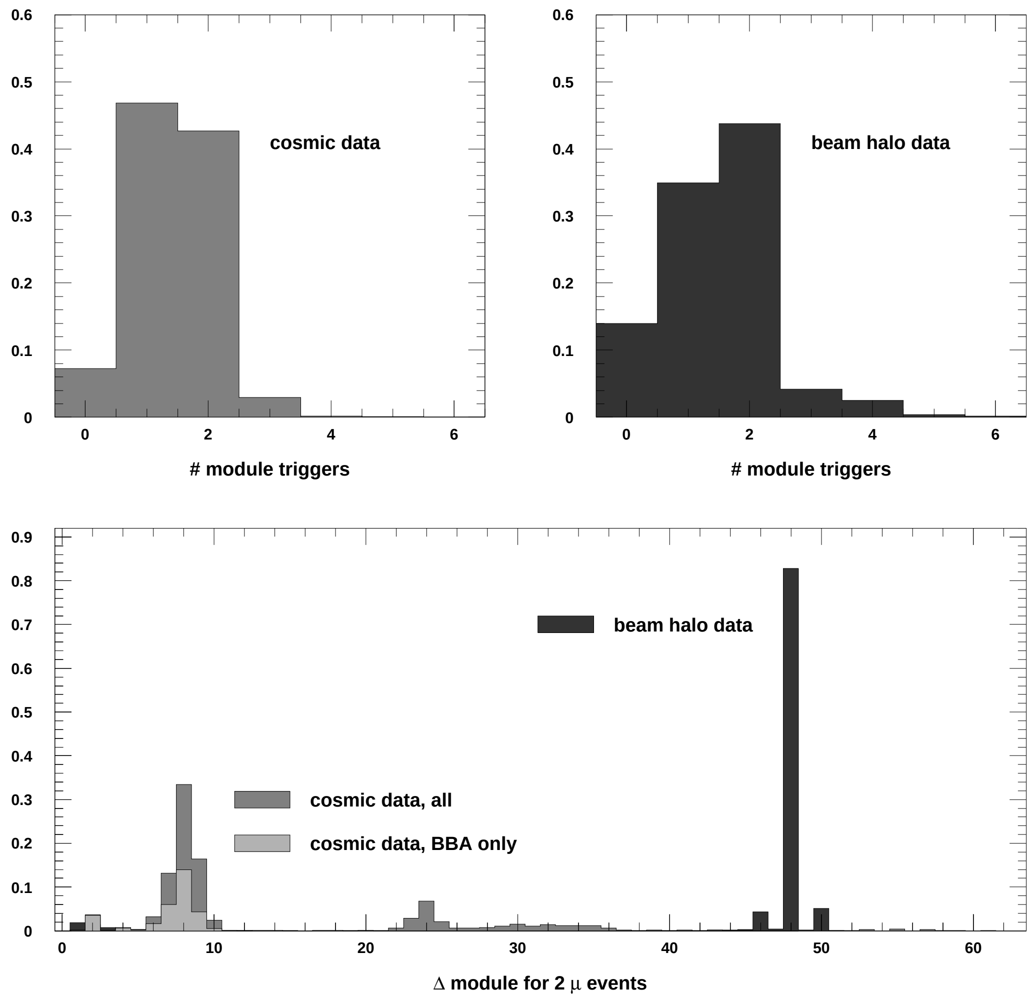

Figure 7.1.: Top left:distribution of number of module triggers in cosmic data
top right: distribution of number of module triggers in beam halo data,
bottom: difference of module numbers for muons events from cosmic radiation and the proton beam halo.

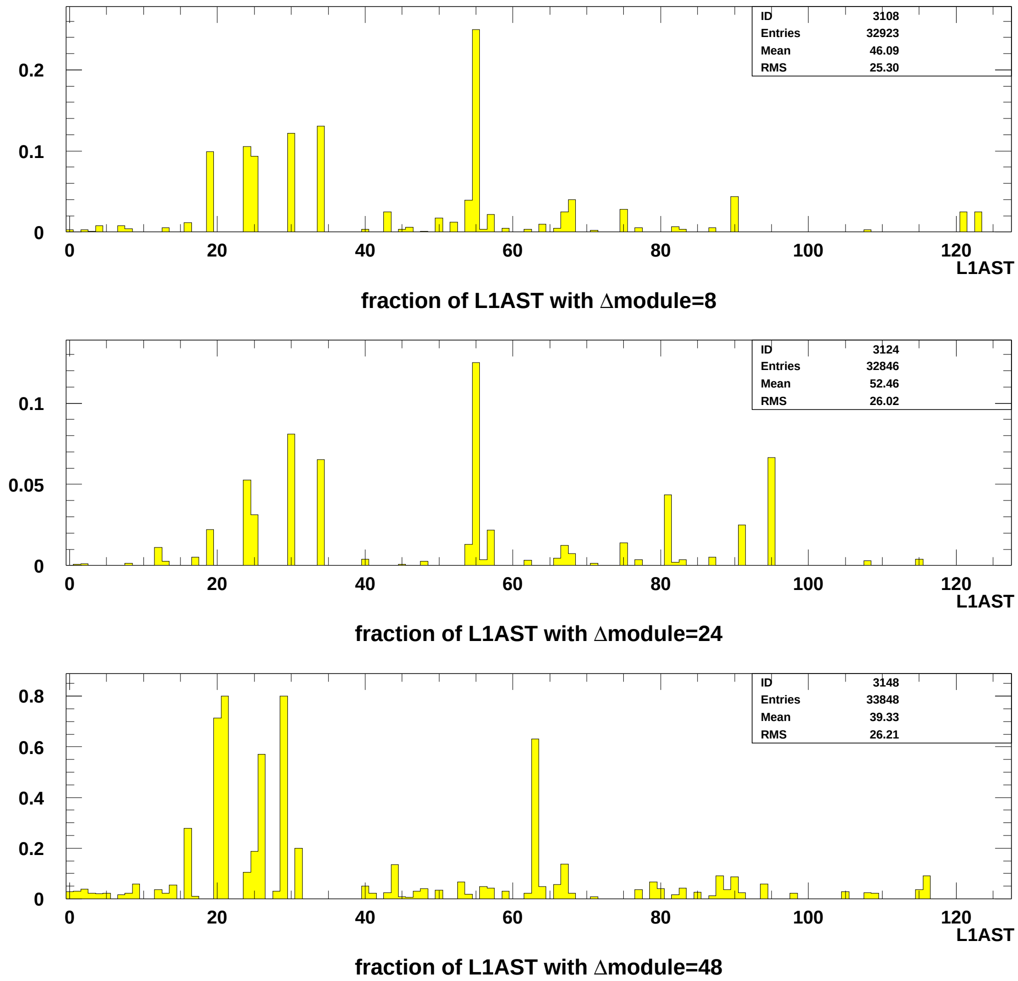

Figure 7.2.: Fractions of L1ASTs fulfilling Δmodule cuts for cosmic and beam halo muons

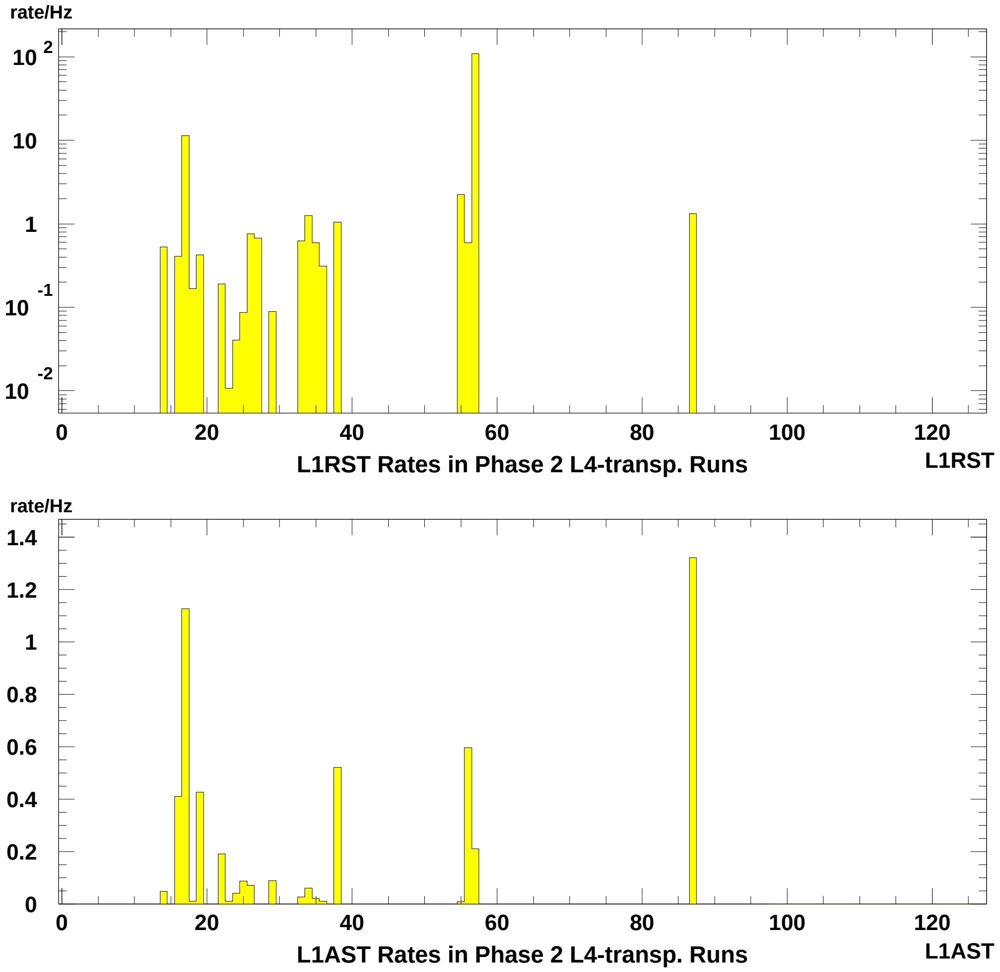

Figure 7.3.: L1RST and L1AST rates phase 2 L4 transparent runs

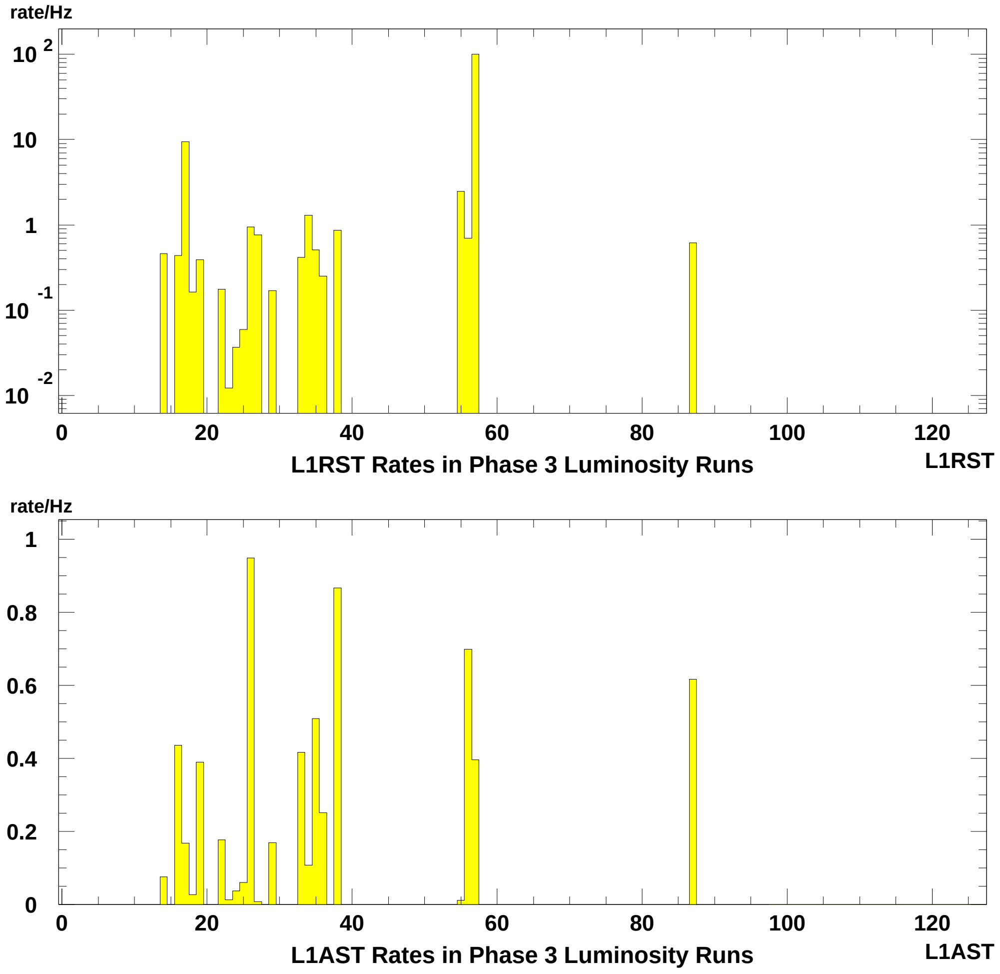

Figure 7.4.: L1RST and L1AST rates phase 3 luminosity runs

8. The Trigger Simulation

The simulation of the Central–μ–Trigger is based on the raw digital wire hit information exclusively. This data is stored in the IRWE (Iron Raw Wire Event) BOS–bank [43]. Due to the separate read out of the information from four single bc after the acceleration of the read out in 1995, a new timeslicewise simulation of the Central–μ–Trigger was possible. The setups of the Layer Boards, Sector Boards and the GPTP Card for all run periods are stored in data base banks which are unpacked within the program package. These banks also serve as steering banks for the online initialisation of the trigger hardware (see appendix F). For example the bank ILCH (Iron Layer Coincidences Hardware Parameters) contains one row with the setup parameters for each Layer Board:

```
%
ILCH 8 / 3 64
   35 16 1     35  0 1    35 17 1    35  1 1
   35 18 1     35  2 1    35 19 1    35  3 1
 2312 20 1   2312  4 1    35 21 1    35  5 1
   35 22 1     35  6 1    35 23 1    35  7 1
   24  8 1     24  9 1    24 10 1    24 11 1
   24 24 1     24 25 1    24 26 1    24 27 1
   24 28 1     24 64 1    24 65 1    24 66 1
   24 67 1     24 68 1    24 69 1    24 12 1
   24 40 1     24 41 1    24 42 1    24 43 1
   24 44 1     24 45 1    24 46 1    24 47 1
   24 48 1     24 70 1    24 71 1    24 72 1
   24 73 1     24 74 1    24 75 1    24 44 1
   35 48 1     35 32 1    35 49 1    35 33 1
   35 50 1     35 34 1    45 51 1    45 35 1
   45 52 1     45 36 1    45 53 1    45 37 1
   35 54 1     35 38 1    35 55 1    35 39 1
%
```

1. column 1 is the identifier of the LUT to be loaded; for example a 35 means the conditions $\geq$3 out of 5, 2312 means : ($\geq$ 1 out of the inner 2) AND ($\geq$ 2 out the outer three layers).

2. column 2 represents the hardware address of the single Layer Board:

$$\begin{aligned} 16 &= 0x10 \sim \text{ cluster 1, Layer Board 0} \qquad (8.1) \\ 67 &= 0x43 \sim \text{ cluster 4, Layer Board 3} \end{aligned}$$

3. column 3 represents the elongation of the ELOR signals in units of bunch crossings.

A second bank ILCD (Iron Layer Coincidences Definitions) contains the logics behind the look–up tables to be downloaded as follows [41]:

```
%
ILCD 2/ 4 60

24  24  24 3      35   56   56 3         ...
24  40  40 3      35  280  280 3         ...
24 264 264 3      35 4120 4120 3         ...
24  48  48 3      35  296  296 3         ...
24 272 272 3      35 4136 4136 3         ...
24 288 288 3      35 4360 4360 3         ...
24   8   8 2      35  304  304 3         ...
24  16  16 2      35 4144 4144 3         ...
24  32  32 2      35 4368 4368 3         ...
24 256 256 2      35 4384 4384 3         ...
                  35    8    8 2         ...
                  35   16   16 2         ...
                  35   32   32 2         ...
                  35  256  256 2         ...
                  35 4096 4096 2         ...
%
```

1. column 1 is the identifier to which refers column 1 of the ILCH bank.
2. if the bitwise Exclusive OR of column 3 and the bitwise AND of the simulated RAM input and column 2 is equal 0, then the (simulated) LB RAM output bit pattern is equal to column 4.

The simulation of the SB and the GPTP is realised analogously to that of the LBs.

To make the trigger simulation as modular as the trigger hardware is, each electronic module is simulated by its appropriate subroutine. The inputs and outputs are transferred in arrays in a common, which also allows a consideration of hardware failures like broken cables etc. or a simulation of new setups by a different cabling.
The software is installed in the //h1util package in patch /trigger and contains the fortran routines listed in table 8. All new/modernised routines need common ITSMC in sequence //h1util/h1util_macros/ironmac. The common represents the cables between the different hardware modules described in chapter 3.

By means of this new trigger simulation it is possible to simulate not only the final Central–μ–TEs, but the output of each electronic unit. In particular it is possible, to simulate timeslicewise the data transmitted to L2/L3. The verification efficiency ε_{ver} then can serve as an indicator of the quality of the system performance. Figures 8.1 and 8.2 show the verification of L1TEs and L2 data (layer coincidence bits) for each module

Name	Purpose
ITSMWB	Simulation of the WDMBs inclusively
ITSMLB	Simulation of the Layer Boards
ITSMSB	Simulation of the Sector Boards
ITSMTP	Simulation of the GPTP–card
ITSMCB	Extracting of the coincidence bits
ITSML1	Simulation of the Triggerelements for bc 0
ITSMTI	Consideration of the module specific t_0 inefficiency
ITSML2	Simulation of the data sent to L2/L3 (the TL23)

Table 8.1.: Central–μ–Trigger Simulation Routines

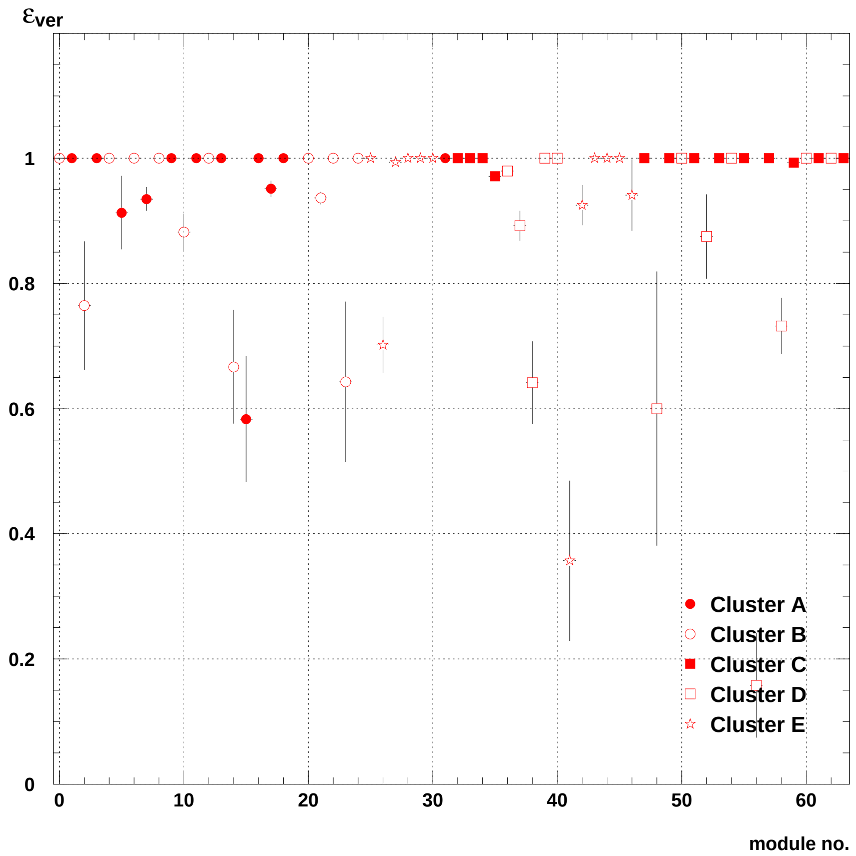

Figure 8.1.: Verification efficiency of L1 triggers from combined cosmic and proton beam halo calibration data

separately from combined cosmic and proton beam halo calibration data. In case of the L1TEs, the 32fold ambiguity of the TE Mu_Bar is resolved (at least to sector level) with the help of the information stored in the monitoring GPTP pipeline. The contents of the pipeline on the L2L3–PQZP–StoreCard is read out for each event and available offline.

Both verification plots show a satisfactory agreement of the simulated and the measured

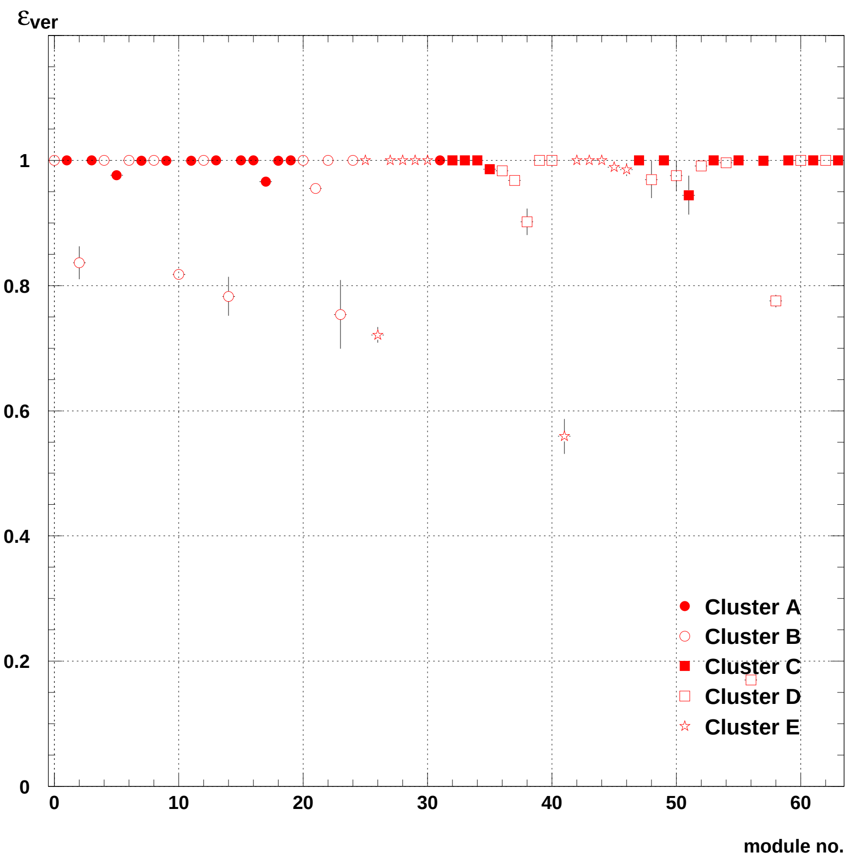

Figure 8.2.: Verification efficiency of L2/L3 data (layer coincidence bits) from combined cosmic and proton beam halo calibration data

data. For the modules with verification efficiencies significantly below 1, the statistics is regrettably low, in particular for the modules mentioned in section 6.2.2.

9. Conclusion

The detailed presentation of the Central–μ–Trigger electronics has shown the complexity and flexibility but also the limits of the Central–μ–Trigger .

The trigger timing, depending sensitively on various system parameters was simulated. From a comparison of the simulated and the measured timing of the Central–μ–Trigger it can be concluded, that its complex behaviour depending on many system parameters is well understood. This includes the knowledge of the reasons for the limited possibility of an optimal calibration.
The flexibility of the Central–μ–Trigger electronics has been proved by its successful application for an H1 BDC trigger, as well as by the given examples for non standard setups for the calibration of other H1 subdetectors
The Central–μ–Trigger simulation enables a fast recognition of anomalies online and the generation of trigger information for Monte Carlo muons.

Part II.

Appendices

A. Glossary

HClk	Digital, symmetric HERA experiment clock, 10.4 MHz $\sim$ 96 ns period
PEn	Pipeline Enable, signal from CTC which enables the filling of the read out pipelines
LnK	Level n Keep, signal from CTC indicating fulfilled condition on trigger level n
LnR	Level n Reject, signal from CTC indicating rejection of the event on trigger level n
FsClr	Fast Clear, signal following the LnR flushing the pipelines before next PEn
FER	Front End Ready, flag from each subdetector that readout is finished which means that system is ready to accept next event.
bc	time unit of one HClk period = 96ns
WDMB	Wire Digital Module Board, the Central–μ–Detector Front End Read Out electronics
WOR	16–fold–Wire–OR of the 16 wire signal from element
LB	Layer Board, processing the WDMB fast trigger output
ELOR	OR of the WOR signals from one trigger layers 3, 4, 5, 8, 12
PLD	Programmable Logic Device
SB	Sector Board, processing the LB output, defines trigger sectors
GPTP	General Purpose Trigger Pipe Board, processing the SB output, defines TEs
t_0	reconstructed time of the ep–interaction
$t_{\rm det}$	time between muon production at the vertex and its detection at the front end electronics
$t_{\rm synch}$	phase of the initial synchronising HClk relative to t_0
$t_{\rm resynch}$	phase of resynchronising HClk relative to signal

B. L1 TEs, L1 STs, L1 Prescale Factors, L2 TEs

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/****************************************/
/**  Definitions of Trigger Elements    **/
/****************************************/

/* ------  TG a -------- LAr T0 ------ TE   0-  7 -----*/

#DEF  LAr_T0           = a t0 b t8 c t9 d t10
#DEF  LAr_electron_1   = a t1
#DEF  LAr_electron_2   = a t2
#DEF  LAr_BT           = a t3
#DEF  LAr_BR           = a t4:2

/* ------  TG b -------- FwdRay ---- TE   8- 15 ------*/

#DEF  FwdRay_T0        = b t0 c t8 d t9
#DEF  FwdRay_Low_Nrw   = b t1
#DEF  FwdRay_Hig_Nrw   = b t2
#DEF  FwdRay_Two_Trk   = b t3
#DEF  FwdRay_Low_Opp   = b t4
#DEF  FwdRay_Low_Side  = b t5
#DEF  FwdRay_Med_Mul   = b t6
#DEF  FwdRay_Hig_Mul   = b t7

/* ------  TG c -------- DCrphi ----- TE  16- 23 -----*/

#DEF  DCRPh_T0         = c t0 d t8
#DEF  DCRPh_Ta         = c t1
#DEF  DCRPh_Tb         = c t2
#DEF  DCRPh_Tc         = c t3
#DEF  DCRPh_TPos       = c t4
#DEF  DCRPh_TNeg       = c t5
#DEF  DCRPh_THig       = c t6
#DEF  DCRPh_TLow       = c t7

/* ------  TG d -------- zvtx  ---- TE  24- 31 ----*/

#DEF  zVtx_T0          = d t0
#DEF  zVtx_T0_nextbc   = d t1
#DEF  zVtx_mul         = d t2:3
/*  0 or 3 and zVtx_T0      zVtx_small   */
/*  0 or 1                  0..5 entries in histo    */
/*  2 or 3                  6..10    */
/*  4                       11..100 entries, peak  1..10    */
/*  5                       11..100 entries, peak  11..255    */
/*  6                       101..x entries (x free, 200 or so)    */
/*  7                       (x+1)..4095 entries    */

#DEF  zVtx_Cls         = d t5
/* all hist. entries within 4 neighbouring bins */

#DEF  zVtx_sig         = d t6:2
/*  0  no significant peak */
/*  1  'sig_1' */
/*  2  'sig_1' and 'sig_new' */
/*  3  'sig_1' and 'sig_new' and 'sig_net' */


/* ------  TG e -------- fwd Muon --- TE  32- 39 ----*/

#DEF  FwdMu_Val_Any        = e t0
#DEF  FwdMu_Val_LRG_ANG    = e t1
#DEF  FwdMu_Val_GT1_SAMOCT = e t2
#DEF  FwdMu_Val_GT1_DIFOCT = e t3
#DEF  FwdMu_Fwd_Vtx        = e t4
#DEF  FwdMu_Pre_Any        = e t5
#DEF  FwdMu_Pre_GT1_SAMOCT = e t6
#DEF  FwdMu_Pre_GT1_DIFOCT = e t7

/* ------  TG f -------- SPCLe ------- TE  40- 47 ----*/

#DEF  SPCLe_IET_Cen_2  = f t0
#DEF  SPCLe_IET_C_9    = f t1
#DEF  SPCLe_IET        = f t3:2
#DEF  SPCLe_IET_Cen_3  = f t5
#DEF  SPCLe_ToF_E_1    = f t6
#DEF  SPCLe_ToF_E_2    = f t7

/* ------  TG g -------- SPCLh ------- TE  48- 55 ---------*/

#DEF  SPCLh_AToF_Cl1   = g t0
#DEF  SPCLh_AToF_E_1   = g t1
#DEF  SPCLh_AToF_E_2   = g t2
#DEF  SPCLe_IET_Hot    = g t3
#DEF  SPCLh_ToF_E_1    = g t4
#DEF  SPCLh_ToF_E_2    = g t5
#DEF  SPCLh_LED        = g t6
#DEF  SPCLh_LED_Flag   = g t7

/* ------  TG h -------- dig Muon --- TE  56- 63 ----*/

#DEF  Mu_BIEC          = h t0
#DEF  Mu_BOEC          = h t1
#DEF  Mu_2_BIoOEC      = h t2
#DEF  Mu_Bar           = h t3
#DEF  Mu_2_Bar         = h t4
#DEF  Mu_FIEC          = h t5
#DEF  Mu_FOEC          = h t6
#DEF  Mu_2_FIoOEC      = h t7

/* ------  TG i -------- ToF (1) veto TE  64- 71  ---*/

#DEF  BToF_IA          = i t0
#DEF  BToF_BG          = i t1
#DEF  BToF_Gl          = i t2
#DEF  PToF_IA          = i t3
#DEF  PToF_BG          = i t4
#DEF  PToF_Gl          = i t5
#DEF  FToF_IA          = i t6
#DEF  FToF_BG          = i t7

/* ------  TG j -------- MWPC ------- TE  72- 79 ---*/

#DEF  Fwd_Cosmic       = j t0
/* DEF  CIP_V            = j t1 */
/* DEF  COP_T0           = j t2 */
/* DEF  Bwd_BR           = j t1 */
/* DEF  Topo_BR          = j t2 */
#DEF  CIP_Backward     = j t3
#DEF  ScBoOr           = j t4
#DEF  CIP_4            = j t5
#DEF  CIP_2            = j t6
#DEF  CIP_Low          = j t7
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/* ------  TG k -------- LAr prov --- TE  80- 87 ---*/

#DEF  LAr_IF           = k t0:2
#DEF  LAr_CB           = k t2:2
#DEF  LAr_FB           = k t4:2
#DEF  LAr_Ebarrel      = k t6:2

/* ------  TG l -------- ---- ------- TE  88- 95 ---*/

#DEF  LAr_BEMC         = l t0:2
#DEF  LAr_EPlug        = l t2:2
#DEF  LAr_FW           = l t4:2
#DEF  LAr_BW           = l t6:2

/* ------  TG m -------- ---- ------- TE  96-103 ---*/

#DEF  LAr_EW           = m t0:4
#DEF  LAr_Etrans       = m t4:2
#DEF  LAr_Etmiss       = m t6:2

/* ------  TG n -------- ---- ------- TE 104-111 ---*/

#DEF RZ_MulMin_6       = n t0
#DEF RZ_MulMin_4       = n t1
#DEF RZ_MulMin_2       = n t2
#DEF RZ_MulMin_1       = n t3
#DEF RZ_non_vtx        = n t4
#DEF RZ_Bwd_COZ_OR     = n t5
#DEF RZ_sig1           = n t7

/* ------  TG o -------- Lumi/eTag -- TE 112-119 ---*/

#DEF  LU_PD_very_low = o t0
#DEF  LU_PD_low      = o t1
#DEF  LU_ET_44       = o t2
#DEF  LU_ET          = o t3
#DEF  LU_PD          = o t4
#DEF  LU_WatVet      = o t5
#DEF  eTAG           = o t6
#DEF  LU_ET_8        = o t7

/* ------  TG p -------- Veto ------- TE 120-127 ---*/

#DEF  FwdScOr            = p t2
#DEF  VETO_inner_BG      = p t3
#DEF  VETO_Outer_BG      = p t4
#DEF  VETO_inner_Global  = p t5
#DEF  VETO_Outer_Global  = p t6


/* ------  TG A -------- Soapbox ------- TE 128-135 ---*/

#DEF  Soap_Pulser        = A t4

/* ------  TG B -------- BDC ------- TE 136-143 ---*/

#DEF  BDC_ANDs_R0        = B t0
#DEF  BDC_ANDs_R1        = B t1
#DEF  BDC_ANDs_R2        = B t2
#DEF  BDC_ANDs_R3        = B t3
#DEF  BDC_ORs_R0        = B t4
#DEF  BDC_ORs_R1        = B t5
#DEF  BDC_ORs_R2        = B t6
#DEF  BDC_ORs_R3        = B t7

/* ------  TG C -------- BackBR ------- TE 144-151 ---*/

#DEF  Bwd_BR       = C t0:4

/* ------  TG D -------- TopoBR ------- TE 152-159 ---*/

#DEF  Topo_b2b      = D t0
#DEF  Topo_0        = D t1
#DEF  Topo_BR       = D t2
#DEF  Topo_Mult     = D t3:4
#DEF  Topo_7        = D t7

/* ------  TG E -------- FPS ------- TE 160-167 ---*/

#DEF  FPS       = E t6

/* ------  TG G -------- FNC ------- TE 176-183 ---*/

#DEF  FNC_Esum      = G t0:4
#DEF  FNC_Moni      = G t4
#DEF  FNC_Tail      = G t5
#DEF  FNC_Finger    = G t6
#DEF  FNC_Hodo      = G t7

/* ------  TG F -------- BPlug ------- TE 184-191 ---*/

#DEF  BPlg_AToF_E_1 = H t0
#DEF  BPlg_AToF_E_2 = H t1
#DEF  BPlg_ToF_E_1  = H t2
#DEF  BPlg_ToF_E_2  = H t3
#DEF  SPCLe_AToF_Cl1   = H t4
#DEF  SPCLe_AToF_E_1   = H t5
#DEF  SPCLe_AToF_E_2   = H t6


/* ------  Abbreviations  --------*/

#SHORT MuMulti #LONG ((Mu_2_BIoOEC+Mu_2_Bar+Mu_2_FIoOEC)>0+(Mu_BIEC+Mu_BOEC+Mu_Bar+M
#SHORT Mu_Any #LONG ((Mu_BIEC+Mu_BOEC+Mu_Bar+Mu_FIEC+Mu_FOEC)>0)
#SHORT Mu_Non_Fwd #LONG ((Mu_BIEC+Mu_BOEC+Mu_Bar+Mu_FOEC)>0)
#SHORT Mu_FEC_BEC #LONG (Mu_BIEC+Mu_BOEC)*(Mu_FIEC+Mu_FOEC)
#SHORT Mu_BEC #LONG (Mu_BIEC+Mu_BOEC)
#SHORT Mu_FEC #LONG (Mu_FIEC+Mu_FOEC)
#SHORT Mu_2_FEC #LONG ((Mu_FIEC+Mu_FOEC)>1||Mu_2_FIoOEC)
#SHORT Mu_2_BEC #LONG ((Mu_BIEC+Mu_BOEC)>1||Mu_2_BIoOEC)
#SHORT Mu_EC #LONG (Mu_BIEC||Mu_BOEC||Mu_2_BIoOEC||Mu_FIEC||Mu_FOEC)
#SHORT Mu_ECQ #LONG (Mu_BOEC||Mu_2_BIoOEC||Mu_FOEC)
#SHORT FwdRay_Topo #LONG (FwdRay_Low_Nrw||FwdRay_Two_Trk||FwdRay_Low_Opp)
#SHORT Ray_T0 #LONG (zVtx_T0||FwdRay_T0)
#SHORT Mu_EC_Barrel #LONG (Mu_BIEC+Mu_BOEC+Mu_FIEC+Mu_FOEC)*Mu_Bar
#SHORT VETO_Or_Global #LONG (VETO_inner_Global||VETO_Outer_Global)
#SHORT FwdMu_Val_Multi #LONG (FwdMu_Val_GT1_SAMOCT||FwdMu_Val_GT1_DIFOCT)
#SHORT Any_Dummy #LONG (BToF_IA||!BToF_IA)
#SHORT DCRPh_T0_VETO_nextbc #LONG (DCRPh_T0&&!zVtx_T0_nextbc)
#SHORT DCRPh_CNH #LONG (DCRPh_Tc&&DCRPh_TNeg&&DCRPh_THig)
#SHORT DIFF_VETO #LONG !FToF_IA && !FwdMu_Fwd_Vtx
#SHORT etag_44 #LONG ( LU_ET_44 && !LU_PD_low && !LU_WatVet )
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#SHORT etag_veto #LONG ( LU_ET_44 || LU_ET )
/* Note that etag is already a similar combination of trigger elements within the Lu
#SHORT etag_all #LONG ( (LU_ET_44 && !LU_PD_low && !LU_WatVet) || eTAG )
#SHORT BDC_Outer_Or #LONG (BDC_ORs_R1||BDC_ORs_R2||BDC_ORs_R3)
#SHORT BDC_And #LONG (BDC_ANDs_R0||BDC_ANDs_R1||BDC_ANDs_R2||BDC_ANDs_R3)
#SHORT BDC_OR #LONG (BDC_ORs_R0||BDC_ORs_R1||BDC_ORs_R2||BDC_ORs_R3)
#SHORT BDC_Any #LONG (BDC_ANDs_R0||BDC_ANDs_R1||BDC_ANDs_R2||BDC_ANDs_R3||BDC_ORs_R0
#SHORT RZ_VETO #LONG (!RZ_non_vtx||RZ_sig1)
#SHORT FT_VETO #LONG (FToF_IA || !FToF_BG)
#SHORT PLUG_VETO #LONG (PToF_IA || !PToF_BG)
#SHORT SPCLe_Low_Thr #LONG (SPCLe_ToF_E_1||SPCLe_IET)
#SHORT zVtx_small #LONG (((zVtx_mul==0)||(zVtx_mul==3)) && zVtx_T0)
#SHORT ZVTX_SUM_0 #LONG ((zVtx_mul==0)||(zVtx_mul==1)) && zVtx_T0
#SHORT ZVTX_SUM_1 #LONG ((zVtx_mul==2)||(zVtx_mul==3))
#SHORT ZVTX_SUM_2 #LONG ((zVtx_mul==4)||(zVtx_mul==5))
#SHORT ZVTX_SUM_3 #LONG (zVtx_mul==6)
#SHORT zVtx_Mu #LONG (((zVtx_mul==0)||(zVtx_mul==3)) && zVtx_T0)||zVtx_sig)
#SHORT zVtx_SNET #LONG (zVtx_sig==3)


#FILE File


/****************************************/
/** Subtrigger                         **/
/**     Physics (P[..]):               **/
/**        P[0]: Physics               **/
/**        P[1]: Monitor               **/
/**       (suppressed if PHYSICS ONLY  **/
/**        selected)                   **/
/**                                    **/
/**     Classification (C[..]):        **/
/**        C[1]: LAr                   **/
/**        C[2]: SpaCal                **/
/**        C[3]: Tracker               **/
/**        C[4]: etag, timing          **/
/**        C[5]: Muon, etc.            **/
/**                                    **/
/**     Beam Gates (O[..]):            **/
/**        O[1]: filled proton bunches **/
/**        O[2]: empty bunches         **/
/**        O[3]: pilot bunches         **/
/**               (e exor p)           **/
/**        O[4]: filled bunches e or p **/
/**              with margin +-2       **/
/**              (default)             **/
/****************************************/


#SET 0

/*****************************************/
/* ep Triggers for 1996                  */
/*****************************************/

s0   SPCLe_IET>2                              v:4 f:1          P[0]      C[2]
s1   SPCLe_IET>2                              v:4 z:0 f:1 t:3  P[0]      C[2] C[3]
s2   (SPCLe_IET>1||SPCLe_IET_Cen_2)&&DCRPh_Ta&&zVtx_sig v:4 f:0  P[0]      C[2] C[3]
s3   SPCLe_IET>2 && SPCLe_ToF_E_2             v:4 f:0          P[0]      C[2]
s4   (SPCLe_IET>2||SPCLe_IET_Cen_3)&&SPCLe_ToF_E_2 v:4 f:1 t:3 z:0  P[0]   C[2] C[3]
s5   (SPCLe_IET>1||SPCLe_IET_Cen_2)&&PToF_IA&&LAr_IF>1 v:4 f:0   P[0]      C[1] C[2]

s6   SPCLe_IET>0                              v:4 f:1 t:3 z:0  P[0]      C[2] C[3]
s7   SPCLe_IET_Cen_3&&SPCLe_ToF_E_2           v:4 f:1 z:0      P[0]      C[2] C[3]
s8   (SPCLe_IET>2||SPCLe_IET_Cen_3)&&zVtx_Cls v:4 f:1 z:0      P[0]      C[2] C[3]

s9   SPCLe_IET>1                              v:4 f:1 t:3 z:0  P[0]      C[2] C[3]
s10  SPCLe_IET_Cen_2 && LU_PD                 v:4 f:1 t:8 z:0  P[0]      C[2] C[3]
s11  (SPCLe_IET>1||SPCLe_IET_Cen_2) && (BToF_BG || PToF_BG) v:6 f:0 t:5 r:0   P[1]
s12  SPCLe_IET>1 && LU_PD                     v:4 f:1 z:0      P[0]      C[2] C[3]
s13  (SPCLe_IET>2||SPCLe_IET_Cen_3)&&SPCLe_ToF_E_2 v:0 f:0     P[0]      C[2]

s14  Mu_FOEC && zVtx_small                    v:1 z:1 t:3 f:0  P[0]      C[5]
s15  FwdRay_Topo && Mu_FIEC && FwdMu_Pre_Any  v:1 z:1     f:0  P[0]      C[5]
s16  Mu_FIEC && FwdMu_Val_Any                 v:1 z:1 t:3 f:0  P[0]      C[5]
s17  Mu_FIEC && zVtx_small                    v:1 z:1 t:7 f:0  P[0]      C[5]
s18  Mu_ECQ&&DCRPh_Ta&&DCRPh_THig&&zVtx_Cls   v:5 z:2     f:0  P[0]      C[3] C[5]
s19  Mu_Bar&&DCRPh_CNH&&zVtx_sig              v:4 z:2 t:3 f:0  P[0]      C[3] C[5]
s20  Mu_FEC_BEC&&VETO_inner_Global                             P[1]      C[5]
s21  Mu_FEC_BEC&&VETO_Outer_Global                             P[1]      C[5]
s22  Mu_ECQ&&zVtx_sig&&DCRPh_CNH              v:4 z:2 r:0 f:0  P[0]      C[5]
s23  FwdMu_Val_Multi&&Mu_2_FEC                v:5         f:0  P[0]      C[5]
s24  Mu_Any && LAr_Etrans>1                   v:1 z:0 t:3 f:0  P[0]      C[1] C[5]
s25  Mu_Any && LAr_Etmiss>1                   v:1 z:0 t:3 f:0  P[0]      C[1] C[5]
s26  Mu_2_FEC+Mu_2_BEC+Mu_FEC_BEC             v:1 z:4 t:3 f:0  P[0]      C[5]
s27  (Mu_EC_Barrel+Mu_2_Bar)&&DCRPh_Ta        v:1 z:2 t:3 f:0  P[0]      C[3] C[5]
s28  FwdMu_Val_Multi                          v:0 z:2 t:3 f:0  P[0]      C[5]
s29  FwdMu_Val_Any&&(Mu_FOEC+Mu_Bar+Mu_BEC)   v:1 z:2 t:3 f:0  P[0]      C[5]
s30  Mu_Bar && CIP_4                                           P[1]      C[5]
s31  Mu_FEC&&BToF_BG                                           P[1]      C[5]

s32  zVtx_sig&&DCRPh_Tc                       v:1         f:0  P[0]      C[3]

s33  FwdRay_Topo && Mu_FIEC && FwdMu_Pre_Any && DCRPh_CNH && zVtx_sig  v:1 z:1     f
s34  Mu_Bar && DCRPh_Ta&&DCRPh_TNeg&&DCRPh_THig && (zVtx_small || zVtx_Cls)  v:4 z:2

s35  Mu_Bar&&DCRPh_CNH&&RZ_sig1               v:4 r:1 t:3 f:0  P[0]      C[3] C[5]
s36  Mu_ECQ&&RZ_sig1&&DCRPh_CNH               v:4 t:0 r:1 f:0  P[0]      C[5]
s37  zVtx_SNET&&DCRPh_CNH&&LAr_BR             v:0 r:0 f:0      P[0]      C[3] C[1]
s38  FwdRay_Topo&&Mu_FIEC&&DCRPh_Ta&&DCRPh_THig&&zVtx_Cls  v:4 z:1 r:3 f:0 P[0]

s43  eTAG && zVtx_sig && DCRPh_Ta && Bwd_BR    v:1 f:0 t:0 r:3  P[0]      C[3] C[4]
s44  eTAG && zVtx_sig && DCRPh_Tc && Bwd_BR    v:0 f:0 t:0      P[0]      C[3] C[4]

s49  CIP_4                                     v:0     t:0 f:0  P[1]      C[3]

s50  eTAG && (SPCLe_IET>1||SPCLe_IET_Cen_2)    v:0 f:1     r:3  P[0]      C[3] C[4]
s51  etag_all && (SPCLe_IET>1||SPCLe_IET_Cen_2) && zVtx_Cls && DCRPh_Ta v:0 f:1
s52  zVtx_Cls && DCRPh_TNeg&&LAr_BR&&Topo_Mult<3   v:1 r:0 f:0  P[0]      C[3] C[1]
s53  zVtx_SNET&&DCRPh_CNH&&SPCLe_ToF_E_1&&Bwd_BR>1 v:1 r:0 f:0  P[0]      C[3]
s54  zVtx_Cls && DCRPh_TNeg && DCRPh_THig && Topo_BR  v:1 f:0   P[0]      C[3]

s55  Mu_Bar&&CIP_4&&DCRPh_Ta&&!LAr_EPlug&&!LAr_IF v:1     f:0   P[0]      C[3] C[5]

s56  (LAr_CB+LAr_FB)&&DCRPh_TNeg&&LAr_BR       v:4 t:0 f:1 r:1  P[0]      C[1] C[3]
s57  zVtx_sig&&DCRPh_Tc&&LAr_BR                v:1     f:1 f:0  P[0]      C[1] C[3]

s59  RZ_sig1&&RZ_MulMin_2&&DCRPh_CNH&&SPCLe_ToF_E_1&&LAr_BR&&FwdMu_Fwd_Vtx  v:0 t:0

s60  LAr_EW&&DCRPh_Ta                          v:4 t:3 f:1 r:5  P[0]      C[1] C[3]

s62  SPCLe_IET>1 && LU_PD_very_low             v:4 f:1 t:8 z:0  P[0]      C[2] C[3]
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s63  FwdMu_Val_Any&&VETO_Or_Global                               P[1]      C[5]

s64  LAr_Etrans>2 && LAr_IF>1                  v:4 r:5 f:1 t:8 l:0 P[0]      C[1]
s66  LAr_Etmiss>2 && LAr_IF>1                  v:4 f:0 t:8 l:0   P[0]      C[1]
s67  LAr_electron_2                            v:4 f:0 t:8 l:0   P[0]      C[1]
s68  LAr_IF==0&&Topo_Mult==2&&!FwdMu_Fwd_Vtx&&DCRPh_Ta&&zVtx_Cls v:0   P[0]    C[1]

s71  LAr_Etmiss && DCRPh_Ta                    v:0 r:0 f:0 t:3 l:0   P[0]      C[1]
s74  LAr_EW&&DCRPh_Ta&&zVtx_sig                v:1 r:0 f:0           P[0]      C[1]
s75  LAr_electron_1                            v:0 r:0 f:0 t:3 l:0   P[0]      C[1]
s76  LAr_Etrans>1 && CIP_2                     v:0     t:3 f:0 r:7 l:0 P[0]      C[1
s77  LAr_Etmiss>1                              v:0 r:0 f:0 t:3 l:0   P[0]      C[1]
s78  LAr_CB&&DCRPh_Tb                          v:1 r:0 f:0 t:3 l:0   P[0]      C[1]
s79  LAr_FB&&DCRPh_Tb                          v:1 r:0 f:0 t:3 l:0   P[0]      C[1]

s80  etag_all                                  v:0 f:0 t:0       P[0]      C[4]
s81  etag_all&&(SPCLe_IET>1||SPCLe_IET_Cen_2)  v:0 f:1     r:3   P[0]      C[3] C[4]
s82  etag_all && LAr_BR && DCRPh_TNeg          v:4 f:0 t:0 r:3   P[0]      C[1] C[4]
s83  eTAG && zVtx_sig && DCRPh_Tc              v:1 f:0 t:0 r:3   P[0]      C[3] C[4]
s84  etag_44 && zVtx_sig && DCRPh_Tc           v:1 f:0 t:0 r:3   P[0]      C[3] C[4]
s85  etag_all && DCRPh_TNeg                    v:0 f:0 t:0       P[0]      C[3] C[4]
s86  eTAG                                                        P[1]      C[4]
s87  etag_all && DCRPh_Ta && Mu_Any            v:1 f:0 t:0       P[0]      C[3] C[4]
s88  eTAG && DCRPh_T0_VETO_nextbc              v:0 f:0 d:0       P[0]      C[3] C[4]
s89  eTAG && FNC_Esum && DCRPh_Ta              v:0 f:0           P[0]      C[3] C[4]
s90  LU_ET_44                                                    P[1]      C[4]

s91  LU_PD_low                                                   P[1]      C[4]
s92  LU_PD&&!LU_WatVet                                           P[1]      C[4]
s93  LU_WatVet                                                   P[1]      C[4]
s94  LU_ET && LU_PD && !LU_WatVet                                P[1]      C[4]
s95  LU_ET && LU_PD && LU_WatVet                                 P[1]      C[4]

s96  BToF_IA                                                     P[1]      C[4]
s97  BToF_BG                                                     P[1]      C[4]
s98  BToF_Gl                                                     P[1]      C[4]
s99  LU_ET_8                                                     P[1]      C[4]

s100 CIP_Backward                                                P[1]      C[4]
s101 SPCLe_AToF_Cl1                                              P[1]      C[2]

s104 zVtx_T0                                                     P[1]      C[3]
s105 etag_all&&SPCLe_ToF_E_1                   v:4 f:0   r:3     P[0]      C[3] C[4]
s106 FPS && etag_all && DCRPh_Ta               v:0               P[0]      C[3] C[4]
s107 FPS && DCRPh_TNeg                         v:0     t:0       P[0]      C[3] C[4]

s109 FwdRay_T0                                 v:0 f:0           P[1]      C[3]
s110 SPCLe_IET_Hot                             v:0 f:0           P[1]      C[2]
s111 SPCLe_IET>1                               v:0 f:0           P[1]      C[2]

s113 DCRPh_T0                                                    P[1]      C[3]

s115 FNC_Esum>1 && SPCLe_IET>1                 v:0 f:1           P[0]      C[2] C[4]

/* Pilot Bunch triggers */
s116 Any_Dummy                                 v:0     t:0       P[1] O[3] C[4]
s117 DCRPh_TNeg                                v:0 f:0 t:0 r:3   P[1] O[3] C[3]
s118 LAr_BR && CIP_2                           v:0 f:0 t:0       P[1] O[3] C[1] C[3]

/* Provisional special gating */
s121 SPCLh_LED                                                        O[0] C[2]
s123 FNC_Moni

/* Empty Bunch triggers , i.e. cosmics e.g. s124 Gayler Trigger */
s124 Mu_Bar                                        t:0           P[1] O[2] C[5]
s125 DCRPh_Ta && CIP_4                                           P[1] O[2] C[3]
s126 Fwd_Cosmic                                                  P[1] O[2] C[3]
s127 CIP_4 && ScBoOr                                             P[1] O[2] C[3]

#GLOBAL v:0 !BToF_BG
#GLOBAL v:1 !BToF_BG&&!CIP_Backward
#GLOBAL v:2 !BToF_BG&&!SPCLh_AToF_Cl1
#GLOBAL v:3 !BToF_BG&&!SPCLh_AToF_Cl1&&!SPCLe_AToF_E_1&&!VETO_Outer_BG
#GLOBAL v:4 !BToF_BG&&!VETO_inner_BG&&!VETO_Outer_BG
#GLOBAL v:5 !BToF_BG&&!VETO_inner_BG&&!VETO_Outer_BG&&!CIP_Backward
#GLOBAL v:6 !VETO_inner_BG&&!VETO_Outer_BG

#GLOBAL z:0 zVtx_mul<7
#GLOBAL z:1 zVtx_Mu&& zVtx_mul<7
#GLOBAL z:2 zVtx_Mu
#GLOBAL z:3 zVtx_mul
#GLOBAL z:4 zVtx_small

#GLOBAL t:0 zVtx_T0
#GLOBAL t:1 zVtx_T0||LAr_T0
#GLOBAL t:2 zVtx_T0||DCRPh_T0_VETO_nextbc
#GLOBAL t:3 Ray_T0
#GLOBAL t:4 Ray_T0||DCRPh_T0_VETO_nextbc||LAr_T0
#GLOBAL t:5 Ray_T0||DCRPh_T0_VETO_nextbc
#GLOBAL t:6 FwdRay_T0&&!FwdRay_Low_Nrw
#GLOBAL t:7 FwdRay_T0
#GLOBAL t:8 Ray_T0||LAr_T0

#GLOBAL d:0 DCRPh_T0

#GLOBAL l:0 LAr_T0

#GLOBAL f:0 FToF_IA || !FToF_BG
#GLOBAL f:1 (FToF_IA || !FToF_BG) && PLUG_VETO

#GLOBAL r:0 RZ_VETO
#GLOBAL r:1 !RZ_non_vtx
#GLOBAL r:2 !SPCLe_AToF_E_1 && !SPCLh_AToF_E_1
#GLOBAL r:3 !SPCLe_AToF_E_1
#GLOBAL r:4 !SPCLh_AToF_Cl1&&!SPCLe_AToF_E_1
#GLOBAL r:5 RZ_VETO && !SPCLe_AToF_E_1
#GLOBAL r:6 !RZ_non_vtx && !SPCLe_AToF_E_1 && SPCLe_ToF_E_1
#GLOBAL r:7 !RZ_non_vtx && !SPCLe_AToF_E_1

#NEXT_SET 1

/*****************************************/
/* Calibration Triggers for 1996         */
/*****************************************/

s0 Mu_BIEC                                          v:2 z:1 t:6 d:0 l:0 f:1 m:1
s1 Mu_BOEC                                          v:2 z:1 t:6 d:0 l:0 f:1 m:1
s2 Mu_2_BIoOEC                                      v:2 z:1 t:6 d:0 l:0 f:1 m:1
s3 Mu_Bar                                           v:2 z:1 t:6 d:0 l:0 f:1 m:1
s4 Mu_2_Bar                                         v:2 z:1 t:6 d:0 l:0 f:1 m:1
s5 Mu_FIEC                                          v:2 z:1 t:6 d:0 l:0 f:1 m:1
s6 Mu_FOEC                                          v:2 z:1 t:6 d:0 l:0 f:1 m:1
```

```
s7 Mu_2_FIoOEC                                    v:2 z:1 t:6 d:0 l:0 f:1 m:1

s8  Mu_FEC                                        v:3 z:1 t:5 d:0 l:0 f:1 m:1
s9  Mu_BEC                                        v:3 z:1 t:5 d:0 l:0 f:1 m:1

s10  Mu_FEC                                       v:4 z:1 t:5 d:0 l:0 f:1 m:1
s11  Mu_BEC                                       v:4 z:1 t:5 d:0 l:0 f:1 m:1

s12 Mu_Bar&&Mu_EC                                 v:2 z:1 t:6 d:0 l:0 f:1 m:1
s13  Mu_FEC_BEC                                   v:2 z:1 t:6 d:0 l:0 f:1 m:1
s14  Mu_BEC*Mu_Bar                                v:2 z:1 t:6 d:0 l:0 f:1 m:1
s15  Mu_FEC*Mu_Bar                                v:2 z:1 t:6 d:0 l:0 f:1 m:1

s18  Soap_Pulser

s20  Mu_FEC_BEC&&VETO_inner_Global
s21  Mu_FEC_BEC&&VETO_Outer_Global

s23  FwdMu_Val_Any&&Fwd_Cosmic
s24  FwdMu_Val_Any                                v:0     t:3
s25  FwdMu_Val_Multi                              v:0     t:3
s26  FwdMu_Val_Any                                v:3 m:2
s27  FwdMu_Val_Any                                v:4 m:2

s28  VETO_inner_Global && PToF_Gl
s29  BToF_Gl && PToF_Gl
s30  Fwd_Cosmic && BToF_Gl
s31  PToF_IA && FToF_IA && VETO_inner_BG

s32  CIP_4 && BToF_Gl
s33  CIP_2 && BToF_Gl
s34  CIP_2 && Mu_BIEC
s35  CIP_2 && Mu_BOEC
s36  CIP_2 && Mu_BEC
s37  BToF_Gl
s38  BToF_BG
s39  CIP_2

s40  CIP_Low
s41  CIP_Low && Fwd_Cosmic
s42  CIP_Low && ScBoOr
s43  CIP_Low && FwdRay_T0

s46  VETO_Or_Global
s47  BToF_BG && PToF_IA
s48  Fwd_Cosmic && Mu_EC
s49  CIP_4

s50  CIP_4 && DCRPh_Ta
s51  CIP_4 && Mu_Bar
s52  CIP_4 && !BToF_IA
s53  CIP_4 && !SPCLe_ToF_E_1
s54  CIP_2 && Mu_FEC
s55  CIP_2 && Mu_FEC && Fwd_Cosmic
s56  CIP_2 && Mu_FIEC
s57  CIP_4 && Mu_Bar
s58  CIP_2 && Mu_BEC
s59  CIP_4 && zVtx_T0

s60  DCRPh_Ta && DCRPh_T0_VETO_nextbc             v:0         f:0
s61  zVtx_sig                                    v:0         f:0
s62  CIP_2 && Fwd_Cosmic
s63  CIP_2 && VETO_Outer_Global

s64  LAr_Etrans>0                                 v:1     t:3 l:0 m:0
s65  LAr_Etmiss>0                                 v:1     t:3 l:0 m:0
s66  LAr_EW>0                                     v:1     t:3 l:0 m:0
s67  LAr_BT                                       v:1     t:3 l:0 m:0
s68  LAr_IF==0&&Topo_Mult==1&&!FwdMu_Fwd_Vtx&&!RZ_Bwd_COZ_OR   v:0

s70  LAr_IF>0                                 v:1 t:5 l:0 m:0
s71  LAr_IF>1                                 v:1 t:5 l:0 m:0
s72  LAr_IF>2                                 v:1 t:5 l:0 m:0
s73  LAr_Ebarrel>0                            v:1 t:5 l:0 m:0
s74  LAr_Ebarrel>1                            v:1 t:5 l:0 m:0
s75  LAr_Ebarrel>2                            v:1 t:5 l:0 m:0
s76  LAr_Etrans>0                             v:1 t:5 l:0 m:0
s77  LAr_Etrans>1                             v:1 t:5 l:0 m:0
s78  LAr_Etrans>2                             v:1 t:5 l:0 m:0
s79  LAr_Etmiss>0                             v:1 t:5 l:0 m:0
s80  LAr_Etmiss>1                             v:1 t:5 l:0 m:0
s81  LAr_Etmiss>2                             v:1 t:5 l:0 m:0
s82  LAr_EW>0                                 v:1 t:5 l:0 m:0
s83  LAr_EW>1                                 v:1 t:5 l:0 m:0
s84  LAr_EW>2                                 v:1 t:5 l:0 m:0

s85  SPCLe_IET>0 && LU_PD_very_low && !etag_veto v:0 f:2
s86  etag_all && SPCLe_Low_Thr && !SPCLe_AToF_E_2  v:5 f:2
s87  SPCLe_Low_Thr&& !SPCLe_AToF_E_2 &&DCRPh_Ta  v:5 f:2 t:0
s88  SPCLe_IET>1                              v:5 f:2

s90  RZ_MulMin_2                              v:0  t:0
s91  RZ_non_vtx && DCRPh_Ta                   v:0  t:0
s92  RZ_Bwd_COZ_OR && zVtx_small              v:0  t:0
s93  RZ_MulMin_2 && zVtx_small && RZ_sig1  v:0  t:0
s94  RZ_sig1 && (LAr_CB>1)                    v:0  t:0
s95  RZ_sig1 && (LAr_BR>1)                    v:0  t:0

s96  DCRPh_Ta && (LAr_EPlug==0)               v:0  t:0
s97  DCRPh_Ta && !FToF_IA                     v:0  t:0
s98  DCRPh_Ta && !FwdMu_Fwd_Vtx               v:0  t:0
s99  DCRPh_Ta && (LAr_EPlug==0)&&!FToF_IA&&!FwdMu_Fwd_Vtx v:0  t:0
s100 DCRPh_Ta && !FToF_IA && !FwdMu_Fwd_Vtx   v:1  t:0
s101 DCRPh_Ta && !FToF_IA && !FwdMu_Fwd_Vtx && (LAr_EPlug<3) v:1  t:0
s102 DCRPh_Ta && !FToF_IA && !FwdMu_Fwd_Vtx && (LAr_EPlug<2) v:1  t:0

s104 FwdMu_Val_Any
s105 FwdMu_Val_LRG_ANG
s106 FwdMu_Val_GT1_SAMOCT
s107 FwdMu_Val_GT1_DIFOCT
s108 FwdMu_Fwd_Vtx
s109 FwdMu_Pre_Any
s110 FwdMu_Pre_GT1_SAMOCT
s111 FwdMu_Pre_GT1_DIFOCT

s112 eTAG && BToF_IA                           v:0

s113  (LAr_EW>0) && Mu_Any
s114  (LAr_EW>0) && Mu_Bar
s115  (LAr_EW>0) && Mu_FEC_BEC

s116  SPCLe_AToF_Cl1 && Mu_Bar                                   P[1]      C[2] C[5]
```

```
s117  (SPCLe_IET>1||SPCLe_IET_Cen_2) && Mu_Bar                  P[1]      C[2] C[5]
s118  SPCLe_IET
s119  SPCLh_AToF_Cl1

/* used to be Pilot Bunch triggers */
s121 SPCLh_LED                                                       O[0]
s122 SPCLe_IET>1
s123 FNC_Moni

#GLOBAL v:0 !BToF_BG
#GLOBAL v:1 !BToF_BG&&!VETO_inner_BG&&!VETO_Outer_BG
#GLOBAL v:2 VETO_Or_Global
#GLOBAL v:3 VETO_inner_Global
#GLOBAL v:4 VETO_Outer_Global
#GLOBAL v:5 !BToF_BG&&!VETO_inner_BG&&!VETO_Outer_BG

#GLOBAL z:0 zVtx_mul<7
#GLOBAL z:1 zVtx_T0

#GLOBAL t:0 zVtx_T0
#GLOBAL t:1 zVtx_T0||LAr_T0
#GLOBAL t:2 zVtx_T0||DCRPh_T0_VETO_nextbc
#GLOBAL t:3 Ray_T0
#GLOBAL t:4 zVtx_T0||FwdRay_T0||LAr_T0
#GLOBAL t:5 BToF_Gl
#GLOBAL t:6 CIP_2

#GLOBAL d:0 DCRPh_T0

#GLOBAL l:0 LAr_T0

#GLOBAL f:0 FToF_IA || !FToF_BG
#GLOBAL f:1 BToF_Gl
#GLOBAL f:2 (FToF_IA || !FToF_BG) && PLUG_VETO

#GLOBAL m:0 Mu_Any
#GLOBAL m:1 FwdMu_Val_Any
#GLOBAL m:2 (!FwdMu_Pre_GT1_DIFOCT)

#NEXT_SET 3

/*******************************************/
/* Triggers before Lumi Startup (1995)    */
/*******************************************/

s0   SPCLe_IET>2                              v:5 f:1              P[0]      C[2]
s1   SPCLe_IET>2                              v:5 f:1 t:3 r:0      P[0]      C[2]
s2   (SPCLe_IET>1||SPCLe_IET_Cen_2) && DCRPh_THig && zVtx_sig     v:5 f:1
s3   SPCLe_IET>2 && SPCLe_ToF_E_2             v:5 f:1              P[0]      C[2]
s5   SPCLe_IET>1 && PToF_IA && LAr_IF>1       v:5 f:1              P[0]      C[2]

s6   SPCLe_IET>0                              v:5 f:1 t:3          P[0]      C[2]
s7   SPCLe_IET>2                              v:5 f:1              P[0]      C[2]
s8   SPCLe_IET>2 && zVtx_Cls                  v:5 f:1              P[0]      C[2]

s11  SPCLe_IET>1 && (BToF_BG || PToF_BG)      v:6 f:0 t:4 r:0      P[1]      C[2]
s12  SPCLe_IET>1 && LU_PD                     v:5 f:1              P[0]      C[2]
s13  SPCLe_IET>2 && SPCLe_ToF_E_1             v:0 f:1              P[0]      C[2]

s18  Mu_ECQ && DCRPh_Ta                       v:5     t:5          P[0]      C[3]
s19  Mu_Bar && DCRPh_Ta                       v:5     t:5          P[0]      C[3]
s27  (Mu_EC_Barrel+Mu_2_Bar)&&DCRPh_Ta        v:5     t:5          P[0]      C[3]

s64  LAr_Etrans>2                             v:5 z:0 t:0 l:0 d:0  P[0]      C[1]
s65  LAr_EW>2                                 v:5 z:0 t:0 l:0 d:0  P[0]      C[1]
s66  LAr_Etmiss>2                             v:5 z:0 t:0 l:0 d:0  P[0]      C[1]
s67  LAr_electron_2                           v:5 z:0 t:0 l:0 d:0  P[0]      C[1]
s68  LAr_Ebarrel>2                            v:5 z:0 t:0 l:0 d:0  P[0]      C[1]

s72  LAr_Ebarrel>1                            v:5     t:5 l:0      P[0]      C[1]
s73  LAr_EW>1                                 v:5     t:5 l:0      P[0]      C[1]
s75  LAr_electron_1                           v:5     t:5 l:0      P[0]      C[1]
s76  LAr_Etrans>1                             v:5     t:5 l:0      P[0]      C[1]
s77  LAr_Etmiss>1                             v:5     t:5 l:0      P[0]      C[1]

s86  eTAG                                                      P[1]      C[4]
s90  LU_ET_44                                                  P[1]      C[4]
s91  LU_PD_low                                                 P[1]      C[4]
s92  LU_PD&&!LU_WatVet                                         P[1]      C[4]
s93  LU_WatVet                                                 P[1]      C[4]
s94  LU_ET && LU_PD && !LU_WatVet                              P[1]      C[4]
s95  LU_ET && LU_PD && LU_WatVet                               P[1]      C[4]

s96  BToF_IA                                                   P[1]      C[4]
s97  BToF_BG                                                   P[1]      C[4]
s98  BToF_Gl                                                   P[1]      C[4]

s100 CIP_Backward                                              P[1]      C[4]
s101 SPCLe_AToF_Cl1                                            P[1]      C[4]
s102 SPCLh_AToF_Cl1                                            P[1]      C[4]

s110  SPCLe_AToF_Cl1 && Mu_Bar                    v:0          P[1]      C[2] C[5]
s111  (SPCLe_IET>1||SPCLe_IET_Cen_2) && Mu_Bar    v:0          P[1]      C[2] C[5]
s112  SPCLh_ToF_E_1 && Mu_Bar                     v:0          P[1]      C[2] C[5]
s113  SPCLh_AToF_Cl1 && Mu_Bar                    v:0          P[1]      C[2] C[5]

s114 LAr_T0                                                    P[1]      C[1]
s115 LAr_IF>1 && LAr_T0                                        P[1]      C[1]

s117 FNC_Esum>1                                                P[1]      C[4]
s118 FPS                                                       P[1]      C[4]

/* used to be Pilot Bunch triggers */
s121 SPCLh_LED                                                       O[0]
s123 FNC_Moni

#GLOBAL v:0 !BToF_BG
#GLOBAL v:1 !BToF_BG&&!CIP_Backward
#GLOBAL v:3 !BToF_BG&&SPCLh_ToF_E_1&&!SPCLh_AToF_Cl1
#GLOBAL v:4 !BToF_BG&&SPCLh_ToF_E_1&&!SPCLh_AToF_Cl1
#GLOBAL v:5 !BToF_BG&&!VETO_inner_BG&&!VETO_Outer_BG
#GLOBAL v:6 !SPCLh_AToF_Cl1

/* has to be here for technical reasons */
#GLOBAL z:0 zVtx_T0||!zVtx_T0

#GLOBAL t:0 LAr_T0
#GLOBAL t:3 Ray_T0
#GLOBAL t:4 Ray_T0||DCRPh_T0_VETO_nextbc
#GLOBAL t:5 DCRPh_T0_VETO_nextbc

#GLOBAL d:0 DCRPh_T0
```

```
#GLOBAL l:0 LAr_T0

#GLOBAL f:0 !(!FToF_IA&&FToF_BG)
#GLOBAL f:1 (FToF_IA || !FToF_BG) && PLUG_VETO

#GLOBAL r:0 RZ_VETO

#NEXT_SET 4

/******************************************/
/* Gate Test Triggers    */
/******************************************/

s0   Soap_Pulser
s4   Soap_Pulser                                                     O[0]
s8   Soap_Pulser                                                     O[1]
s12  Soap_Pulser                                                     O[2]
s16  Soap_Pulser                                                     O[3]
s20  Soap_Pulser                                                     O[4]

#END_SET
#END_FILE
```

H1 Default prescale factors

Disclaimer:

This produces a list of the current default prescale settings. Note however that for any given run they may be adjusted individually by the shift crew, and that this is frequently being done. The values that have actually been in effect for a given run have to be extracted from the data base bank `ZTPR`.

Subtr	Phase1	Phase2	Phase3	Phase4
0	500	5	2	1
1	100	1	1	1
2	100	2	1	1
3	1	1	1	1
4	100	10	1	1
5	2000	50	1	1
6	1000100	10001	10001	10001
7	3000	40	20	20
8	100	1	1	1
9	1000	100	10	2
10	2000	20	10	1
11	15100	151	151	151
12	100	1	1	1
13	100	1	1	1
14	1000	10	6	1
15	10000	10000	10000	10000
16	100	1	1	1
17	1000	1000	50	6
18	1000	3	1	1
19	100	1	1	1
20	30100	301	301	301
21	400100	4001	4001	4001
22	100	1	1	1
23	100	1	1	1
24	1	1	1	1
25	1	1	1	1
26	1000	10	1	1
27	10000	100	100	100
28	100	1	1	1
29	100	1	1	1
30	30100	301	301	201
31	1000000	10000	10000	7001
32	200000	2000	1000	701
33	2000	50	20	20
34	2000	1	1	1
35	2000	50	1	1
36	2000	50	1	1
37	100000	1000	4	4
38	200	1000	50	1
39	100000	1000	3	1
40	100	1	1	1
41	10000	100	100	100
42	100000	1000	3	1
43	100	45	1	1
44	500	45	1	1
45	200	10	5	2
46	500	100	100	100
47	500	1000	500	500
48	10000	1000	1000	1000
49	16777216	16777216	16777216	16777216
50	2000	20	1	1
51	10000	100	56	5
52	100	6	1	1
53	10000	100	56	5
54	100	6	1	1
55	20000	200	200	150
56	1	1	1	1
57	50000	500	251	10
58	10000	10000	10000	10000
59	100	1	1	1
60	1	1	1	1
61	100	1	1	1
62	100	1	1	1
63	100000	1000	1000	500
64	1	1	1	1
65	100	1	1	1
66	1	1	1	1
67	1	1	1	1
68	500	5	4	1
69	100	1	1	1
70	100	1	1	1
71	1	1	1	1
72	100	1	1	1
73	100	1	1	1
74	10000	100	76	50
75	1	1	1	1
76	3000	30	17	2
77	1	1	1	1
78	20000	200	200	150
79	20000	200	200	150
80	40000	400	300	150
81	10100	101	101	70
82	100	1	1	1
83	100	1	1	1
84	400	10	7	2
85	16100	161	161	161
86	10000100	100001	100001	70001
87	1	1	1	1
88	50000	500	500	300
89	100	1	1	1
90	16777216	600000	250001	150001
91	600000	600000	150001	80001
92	600000	600000	230001	150001
93	2000000	2000000	1000001	1000001
94	100000	100000	50001	50001
95	400000	400000	200001	200001
96	16777216	16777216	16777216	44001
97	16777216	16777216	16777216	16777216
98	13107300	131073	131073	131073
99	10000100	100001	75001	50001
100	16777216	16777216	16777216	16777216
101	16777216	16777216	16777216	16777216
102	16777216	16777216	16777216	16777216
103	5000100	50001	50001	35001
104	16777216	16777216	16777216	16777216
105	100000	1000	1000	1000
106	100	2	1	1
107	10000	1000000	1000000	1000000
108	100	4	2	1
109	5000100	50001	35001	10001
110	16777216	16777216	16777216	16777216
111	16777216	16777216	16777216	16777216
112	16777216	16777216	16777216	16777216
113	16777216	16777216	16777216	16777216
114	100000	1000	3	2
115	100	1	1	1
116	4000100	40001	40001	30001
117	4000100	40001	40001	30001
118	4000100	40001	40001	30001
119	4000100	40001	40001	30001
120	100	1	1	1
121	1	1	1	1
122	100	1	1	1
123	1	1	1	1
124	16777216	3001	3001	3001
125	16777216	3001	3001	3001
126	16777216	16777216	16777216	16777216
127	16777216	16777216	16777216	16777216

Neural Networks (L2NN)

L2 TE	Type	L1 ST	Comment
L2-t0	FF 44	(46,48)	1 x 10 GeV || 2 x 5 GeV Jets
L2-t1	FF 32	(68)	Phi->K+K-, elas., photo
L2-t2	FF 8	(52,54)	J/Psi -> ee el
L2-t3	FF 21	(8)	J/psi/phi/rho in DIS
L2-t4	FF 28	(54)	jpsi->mu+mu-
*L2-t5	FF 40	(19,22)	no nbigray inelastic J/Psi->mu mu
L2-t6	SB 31	(40)	Spacal Back to Back algorithm
*L2-t7	FF 41	(19,22)	inclusive muons
*L2-t8	FF 19	(56,60)	gp->jets
L2-t9	FF 36	(45)	D*
*L2-t10	FF 41	(19,22)	inclusive muons *Copy of L2-t7*
*L2-t11	BG 20	(all)	background - encapsulator

Trigger elements that are presently not rejecting are marked with *.
The following algorithm types are possible: FF: Feed Forward neural net with sigmoidal transfer function, SB: SpaCal Back-to-back pattern recognition, SR: SpaCal Rings, BG: Background Encapsulator.

Topological Trigger (L2TT)

- `L2-t16` SpaCal middle ring (r>10cm roughly, IET>1)
- `L2-t17` SpaCal outer ring (r>20cm roughly, IET>1)
- `L2-t18` QED-Compton (cluster region with IET>1 balanced opposite in phi by cluster region with IET>2) with exclusion of dangerous hot-spot pattern
- `L2-t19` Special outer Spacal region
- `L2-t20` 2 muons (more than 1 digimu or 1 digimu and 2 tracks in Big Rays or Rphi)
- `L2-t21` zVtx analysis : 1 < peak position < 14 .AND. 7 < peak multiplicity < 56
- `L2-t22` 2 or 3 electrons in LAr (above 16 FADC counts)
- `L2-t23` Diffractive Veto (machine is set, if any of the 24 FADC from theta index 0 and 1 of Quickbusses 0 to 3 exceed a predefined threshold of 8 cnts (1 GeV))
- `L2-t24` Cut on zVtx-peak position (active, if 4..12)
- `L2-t25` One and only one module in DgMu .AND. one cluster in LAr-FADC>16 counts in the BTs 2 to 13
- `L2-t26` Two or three well defined clusters in SpaCal IET>1
- `L2-t27` "LAr_electron_2"
- `L2-t28` Two muons back to back in phi: 2 forward big rays *(theta index 2 to 5)* with 1 validated by DgMu
- `L2-t29` Two electrons back to back:
  1. LAr-elma-BT validated by bigray forward and barrel
  2. SpaCal IET>1 backward
  3. 1+2 OR 1+1 OR 2+2 opposite in phi
- `L2-t30` 7 Tof cluster bits in Central Spacal Liet outside hot spot *(x>0, y>0)*
- `L2-t31` BTs in Barrel region unbalanced in phi

For this setup, the SpaCal trigger setup was supposed to be according to the following relations:

- IET>0 *E*>0,5 GeV
- IET>1 *E*>2 GeV
- IET>2 *E*>6 GeV

C. Trigger Element Rates

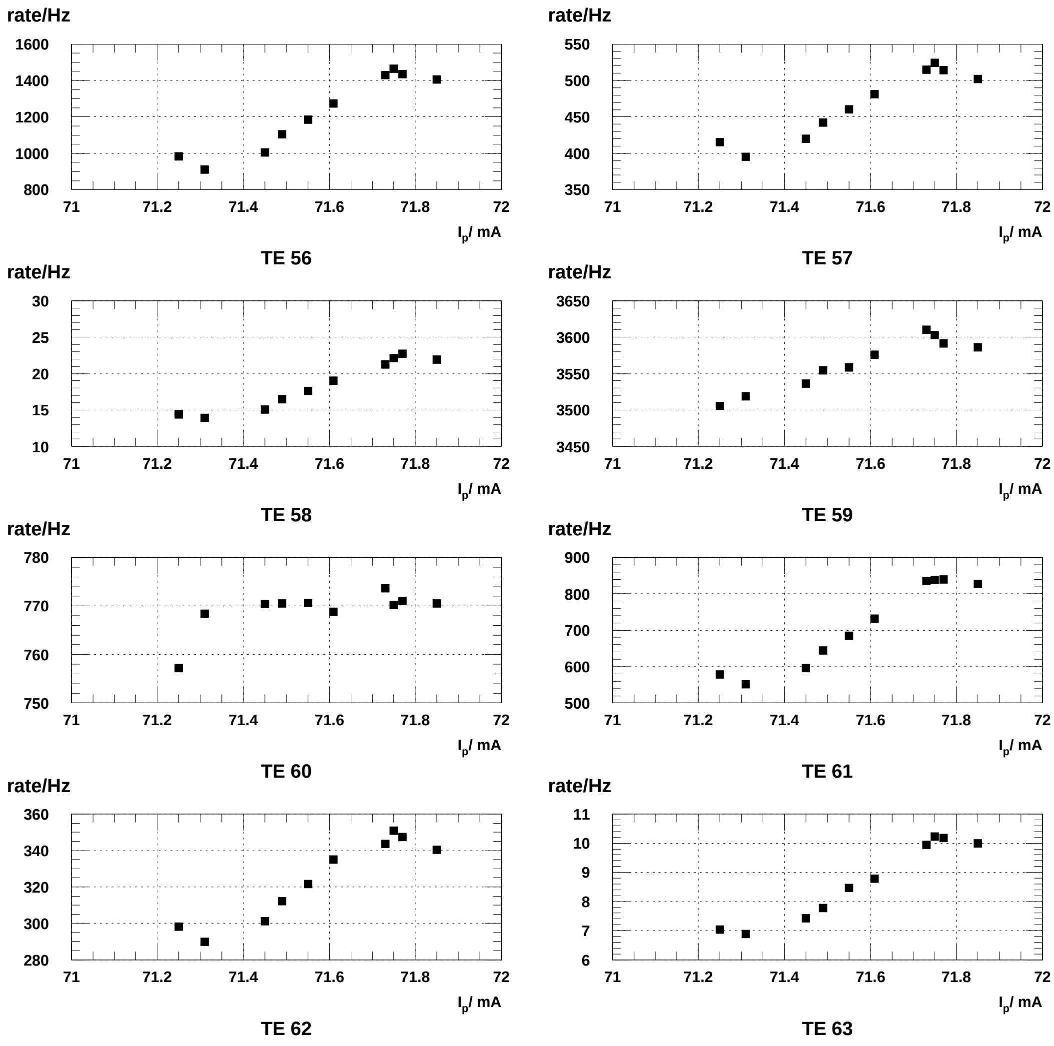

Figure C.1.: Dependency of the Trigger Element Rate on the Proton Beam Current

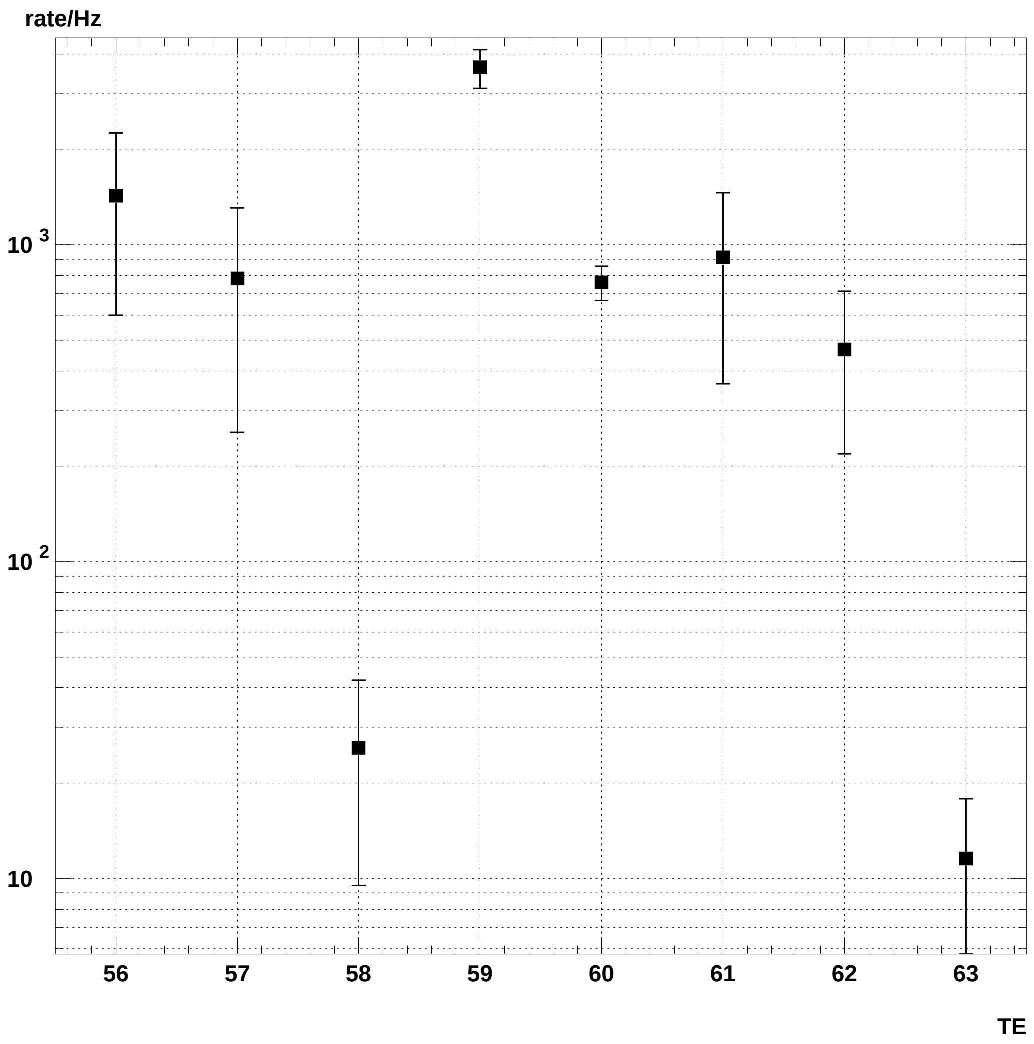

Figure C.2.: Mean Rate of the Central–μ–Trigger Elements

D. Functionality of the WDMB Synchronisation Circuit

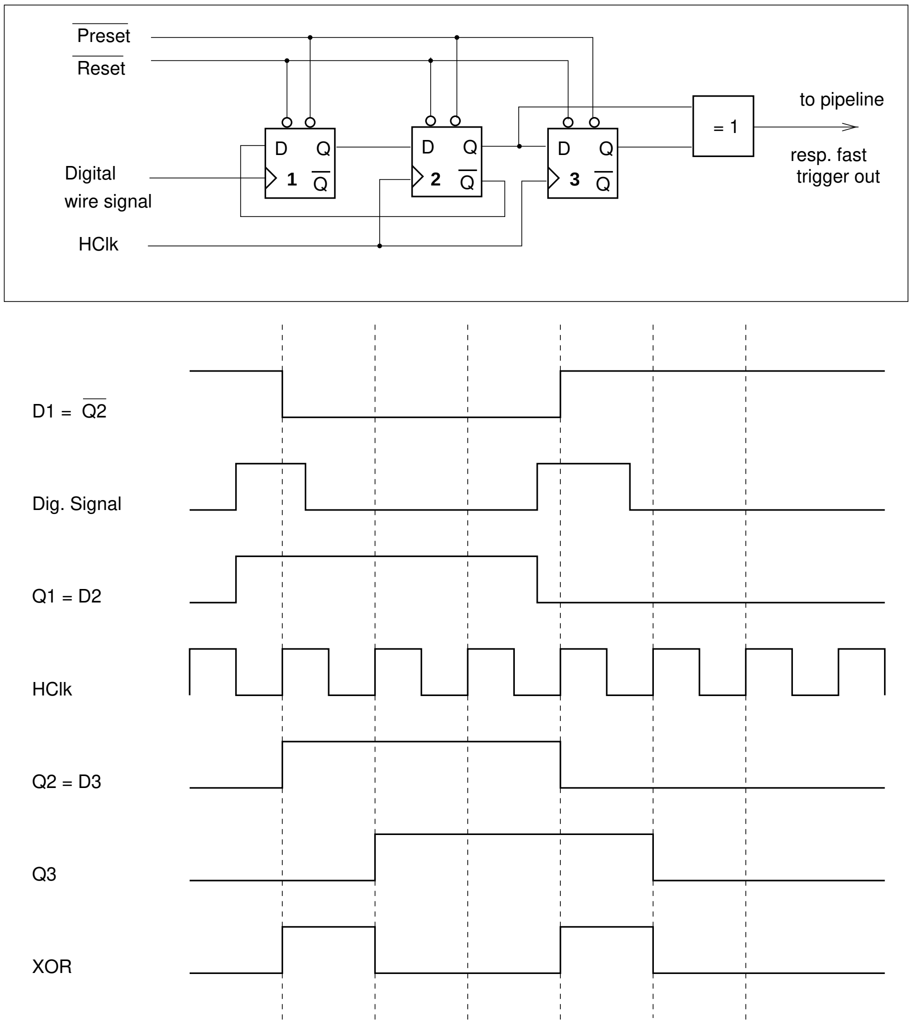

Figure D.1.: The synchronisation of the digitised wire (strip) signals on the WDMB

E. The H1MPSDC in the Central–μ–Trigger

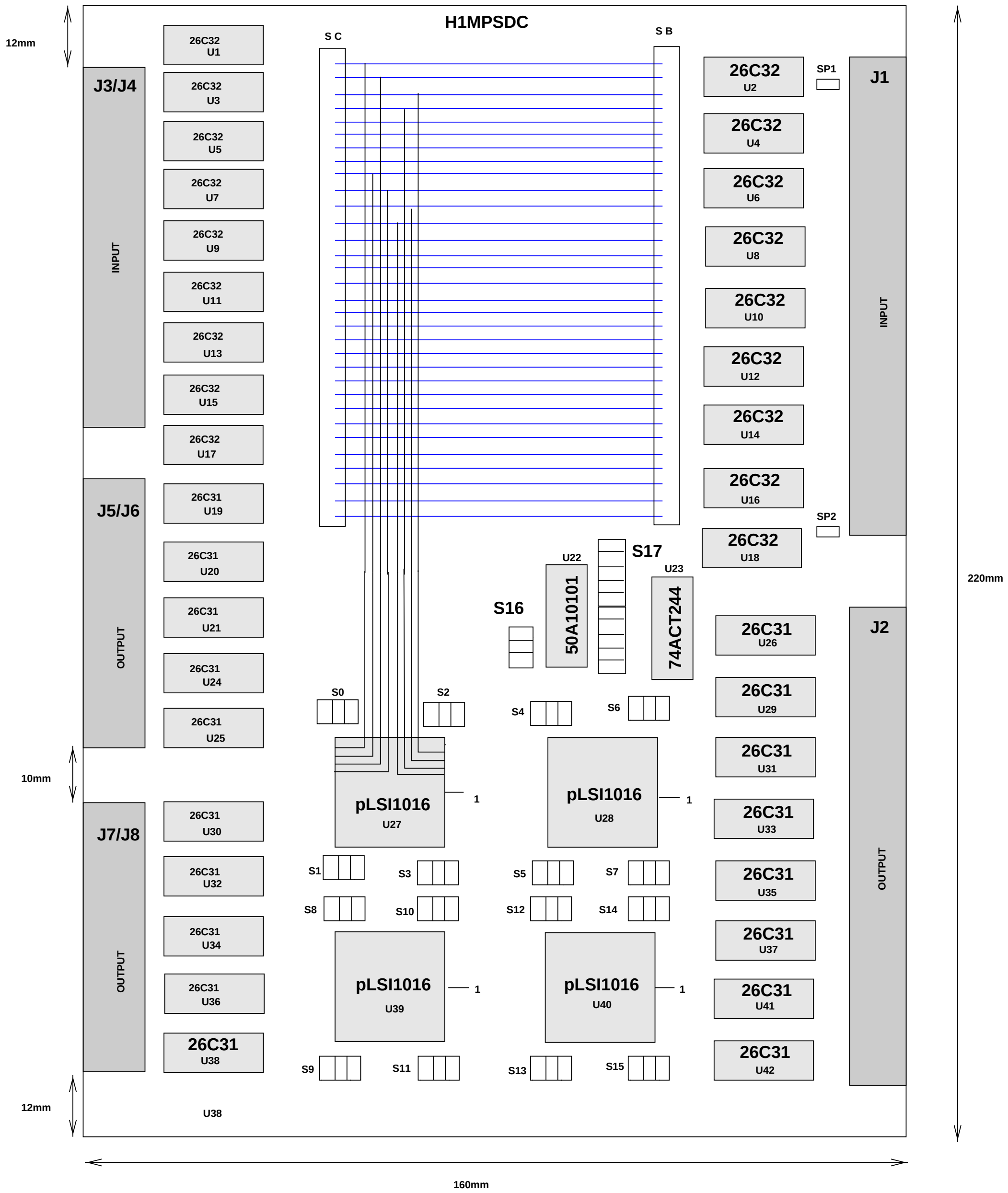

Figure E.1.: Component side view of the H1MPSDC. Top left : input connectors J3–J6 for usage in a standard VME crate (6HU), bottom left output connectors, top right: J1, input connector during usage in the SB crate Jumper SP1, defining the power source line from J1 has to be changed to SP2 during usage in a standard VME crate, bottom right: connectors J7–J10, providing the PLCC output.

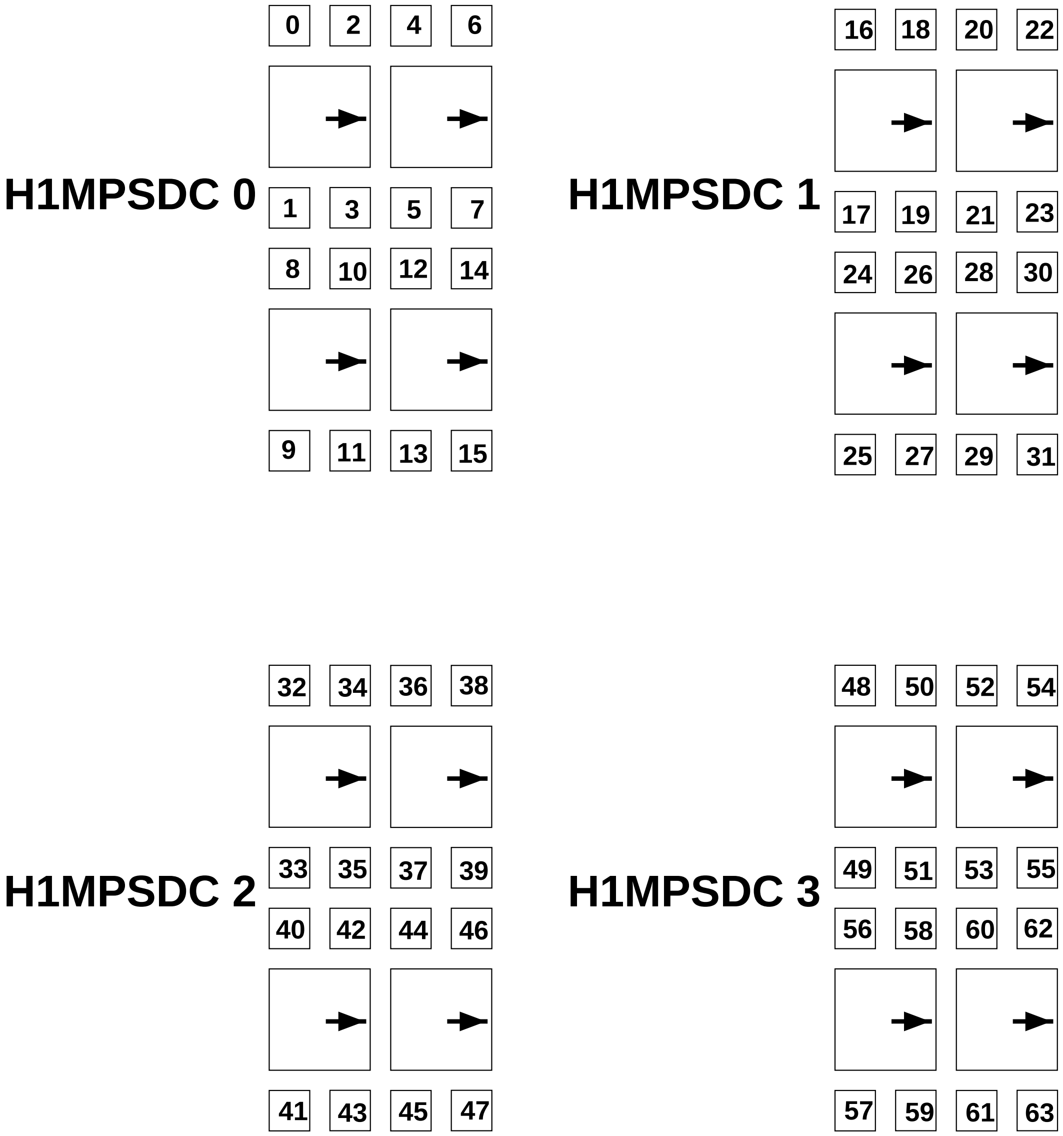

Figure E.2.: Assignment of the LB to the three–bit switches defining the delay on the H1MPSDC

F. Fast Trigger Loading during DAQ

The goals of an online user application which guarantees the intended setup of the different electronic modules of the Central–μ–Trigger during the acquisition of luminosity data are

- security: source of loaded setups is identical to the simulation banks
- flexibililty: possible fast changes of the setups (e.g. for calibration purposes), possible fast action to fix trigger problems from single modules/clusters, hardwareproblems (noise)
- modularity: all three types of boards loadable separately
- comfortability: one button usage; detailed instructions in case of system errors

This is a short description of the ©LabVIEW [42] application, shown in figure F.1. preparing the Central–μ–Trigger electronics for standard data taking. Names of buttons or fields visible on the user interface front panel are written in capitals. A VI (Virtual Instrument) in all contexts here means a LabVIEW Subroutine

F.1. The LAST LOADED Field

This field always indicates date and time of the last successful loading (according to the menu item chosen in the PULL DOWN MENU). When the VI is started date and time are read from file.

F.2. The PULL DOWN MENU

In this menu, the user can choose one of the following four items:

- Reload Everything: all 3 types of boards will be loaded consecutively
- Reload Layer Boards (board type 0)
- Reload Sector Boards (board type 1)
- Reload GPTP (board type 2)

The choice visible while pressing the START button is responsible for the further actions of the program.

Figure F.1.: The Central–μ–Trigger Loading Application

F.3. The MESSAGE Field

This field stays invisible as long as no error occurs (... the OK–LED is green). If unexpectedly something goes wrong, it indicates WHAT has gone wrong and WHY and gives a proposition what to do to cure the problem.

Always try to follow the instructions given in the Message field before you call the (maybe not anymore existing) expert !!!

F.4. The ACTION Field

This text indicator always tells the user, what is going on at the moment. It gets a comment for every step of the loading procedure. When the program has finished properly, it indicates 'Last Correct Reload (see above)'.

F.5. The PROGRESS INDICATOR

For all 3 types of boards the indicator is set to zero. For each cluster of parameters put into the TRIGGER KERNEL VI, the yellow bar (growing from left to right) is incremented by one. Thus, it is NOT indicating the time the program is working already, but the steps of Loading which have already been done.

F.6. The EXPERT PANEL

In general, this panel is hidden beyond the lower border of the Macintosh's screen.

To make it visible and controllable, the (wantstobe) expert first has to enter the password ______________________ and then switch the panel on.

On the left hand side, the VME addresses of the LB–FML, the SB–FML and the GPTP card are controlled. In the center the names and path of the ILCH/ISCH/ITPH banks, on which the entire loading (assignment trigger condition to board) is based, as well as the path of the resulting LUTs are controlled in arrays of strings which are global variables. Via the array of hexadecimals (labelled 'A B C D E') the expert decides whether the LBs in the resp. crate are loaded with the LUT according to the ILCH bank or if they are disabled (loaded with zeros). In addition to this, entire clusters of LBs can be skipped while loading, via the 'CLUSTERS' dip switch array. The latter two features are intended for operation of the system during shutdown periods, in which parts of the detector eventually cannot be read out/initialized/loaded.

F.7. The OK–LED

It is green until an error occurs, then it turns to red and and becomes an ALARM–LED.

F.8. The START Button

Pressing this button triggers the execution of the entire loading procedure. When this boolean control goes true, the choice in the PULL DOWN MENU is checked and loop margins (board types) are set according to the choice. The further progress of the program then is the same for all 3 types of boards:

- loop over board types according to choice in PULL DOWN MENU.
- If the program has not been called on the same day yet, the trigger simulation banks ILCH/ILCD/ISCH/ISCD/ITPH/ITPD are read from the H1 database and all needed LUTs are created. This means, the trigger conditions will be converted into binary files to be loaded into the trigger cards' RAMs.
- Bank name and path for the current board type are put into the VI 'READ BANK' which reads the bank and puts it into a 2D array.
- The board type/2D bank array and the no of rows in the array are put into the VI 'DECODE *current bank name*' which produces an array of clusters (in C: structures) containing the hardware configuration from the bank as well as the full path of the LUT–file to be loaded and the comments for the ACTION field.
- In a loop over all clusters in the array, the contents of each single cluster is put into the VI 'TRIGGER KERNEL' which is the intrinsic interface between the Macintosh and the VME (Loader) cards. For each step the respective action is indicated in the ACTION field, the PROGRESS INDICATOR is incremented.
- If necessary, the error message is written to the MESSAGE field. Program is stopped.

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Lebenslauf

Ich wurde am 9. August 1966 in Hilten, Kreis Grafschaft Bentheim, geboren. Wohnhaft in Uelsen, besuchte ich dort von 1973 bis 1977 die Grundschule und von 1977 bis 1979 die Orientierungsstufe. Von 1979 bis 1983 besuchte ich den Schulzweig Gymnasium der Kooperativen Gesamtschule Neuenhaus. Nach dem Übergang in die Gymnasiale Oberstufe des Gymnasiums Neuenhaus legte ich dort im Sommer 1986 die Abiturprüfungen ab.

Zum Wintersemester 1986/1987 begann ich das Physikstudium an der Rheinisch–Westfälischen–Technischen–Hochschule Aachen. Im Rahmen der H1–Kollaboration am Deutschen Elektronensynchrotron in Hamburg entstand in der Zeit vom Februar 1992 bis Februar 1993 meine Diplomarbeit. Die abschließenden Diplomprüfungen folgten im Juli 1993. Von Juli bis Dezember 1993 war ich als wissenschaftliche Hilfskraft am I. Physikalischen Institut der RWTH Aachen beschäftigt, seit Januar 1994 als wissenschaftlicher Angestellter und arbeite im Rahmen der H1–Kollaboration in Hamburg, das seit Herbst 1993 ist mein vorwiegender Aufenthaltsort ist.
Während der gesamten Zeit meiner Beschäftigung am I. Physikalischen Institut der RWTH Aachen gehörten dazu auch Lehraufgaben.

Heiko Itterbeck

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